

# DOMINO\_BH\_ULT

## Schematics Document

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Title

**Cover Page**

Size

A4

Document Number

**DOMINO BH**

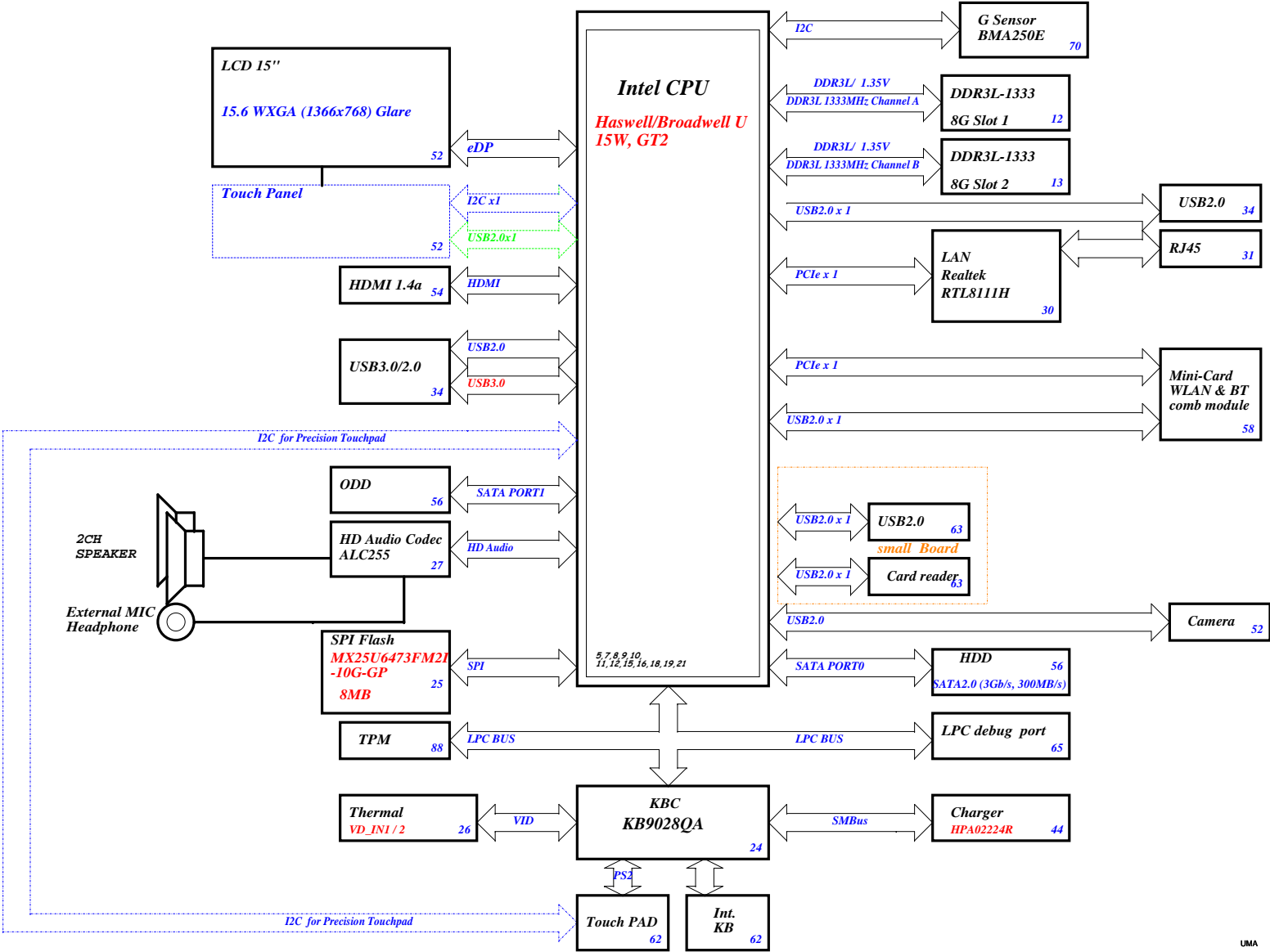
Rev

**-1M**

Date: Friday, December 11, 2015

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Domino\_BH Board Block Diagram



CHARGER		HPA02224	44
INPUTS	OUTPUTS		
19V_DCBATOUT	BT+		
SYSTEM DC/DC		SY8286C_SY8286B	45
INPUTS	OUTPUTS		
19V_DCBATOUT	5V_S5	3D3V_S5	
CPU DC/DC		TPS51624	46-47
INPUTS	OUTPUTS		
19V_DCBATOUT	1V_CPU_CORE		
SYSTEM DC/DC		APW8861	48
INPUTS	OUTPUTS		
19V_DCBATOUT	1D05V_S0		
SYSTEM DC/DC		APW8861	49
INPUTS	OUTPUTS		
19V_DCBATOUT	1D35V_S3		
SYSTEM LDO		S13390D15	51
INPUTS	OUTPUTS		
3D3V_S5	1D5V_S0		

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**CPU (Reserved)**

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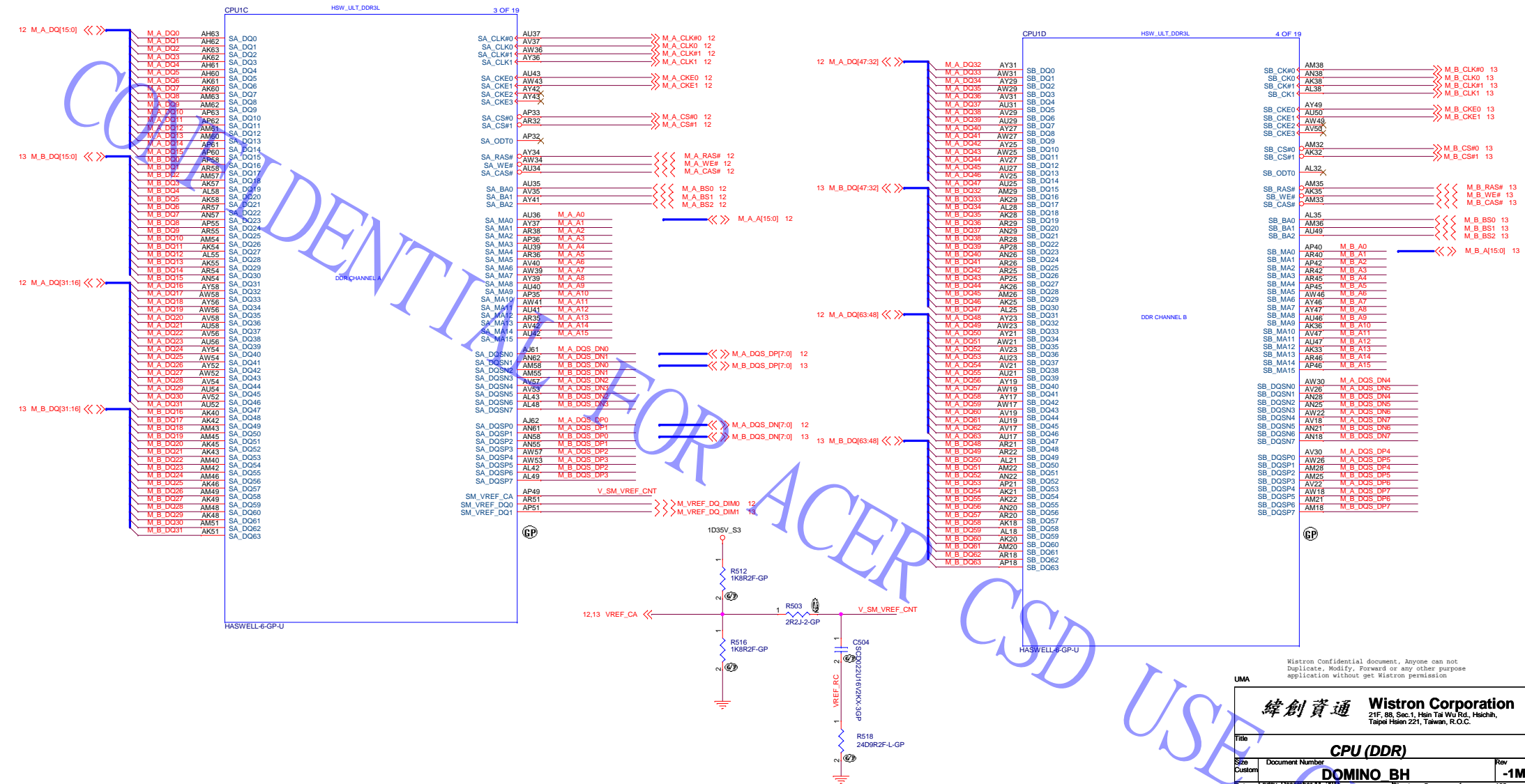
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SSID = CPU



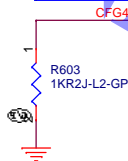
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SSID = CPU

Pin Name	System Pull-up/Pull-down	Schematic Notes	✓
CFG[19:0]		Please refer to the <i>Crescent Bay and (??) Platforms - Debug Port Design Guide (DPDG)</i> .	

Note: Processor strap CFG[4] should be pulled low to enable embedded DisplayPort\*

eDP Enable
CFG4
1: Disable
0: Enable



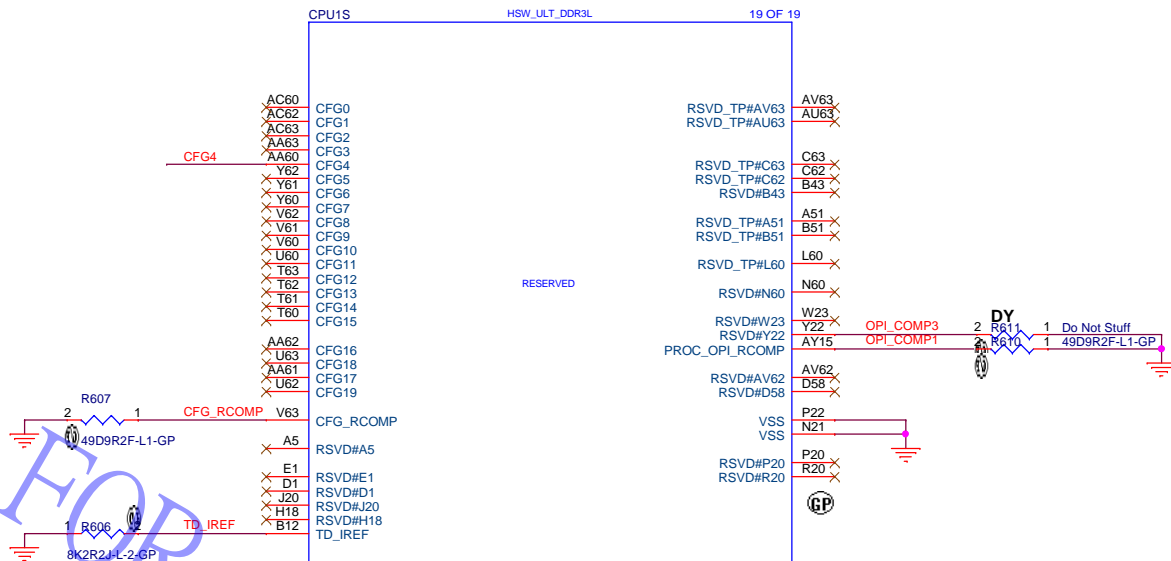
Signal Name	Description	Direction/Buffer Type
CFG[19:0]	<b>Configuration Signals:</b> The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. <ul style="list-style-type: none"><li>CFG[3:0]: Reserved configuration lane. A test point may be placed on the board for these lanes.</li><li>PCI Express* Static x16 Lane Numbering Reversal.</li><li>CFG[4]: eDP enable<ul style="list-style-type: none"><li>1 = Disabled</li><li>0 = Enabled</li></ul></li><li>[19:5]: Reserved configuration lanes. A test point may be placed on the board for these lands.</li></ul>	I/O GTL
CFG_RCOMP	Configuration resistance compensation.	-
FC_x	FC signals are signals that are available for compatibility with other processors. A test point may be placed on the board for these lands. Refer to the appropriate platform design guide for implementation details.	

continued...

## 7.4 Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD - these signals should not be connected
- RSVD\_TP - these signals should be routed to a test point
- RSVD\_NCTF - these signals are non-critical to function and may be left unconnected

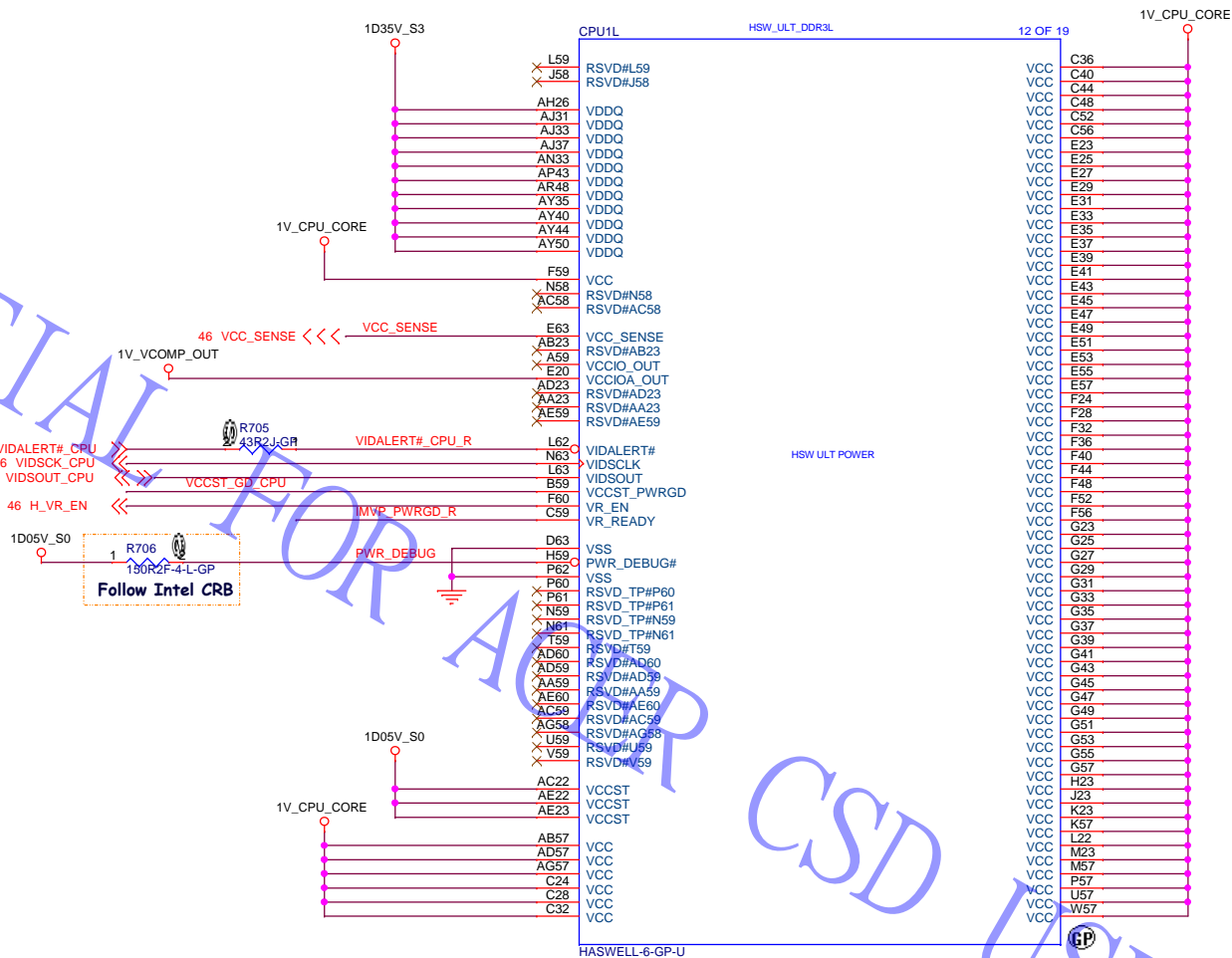
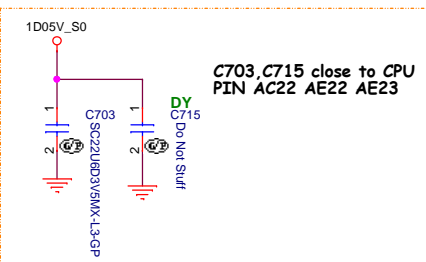
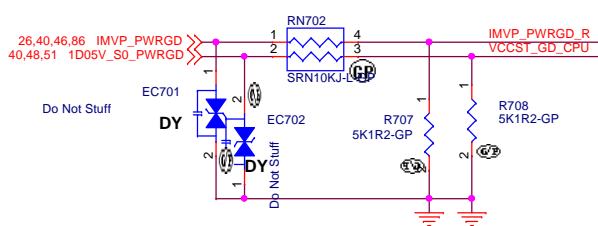
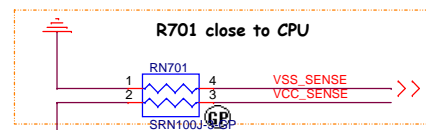
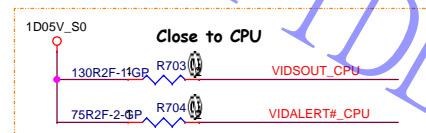


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CPU (CFG)			
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SSID = CPU



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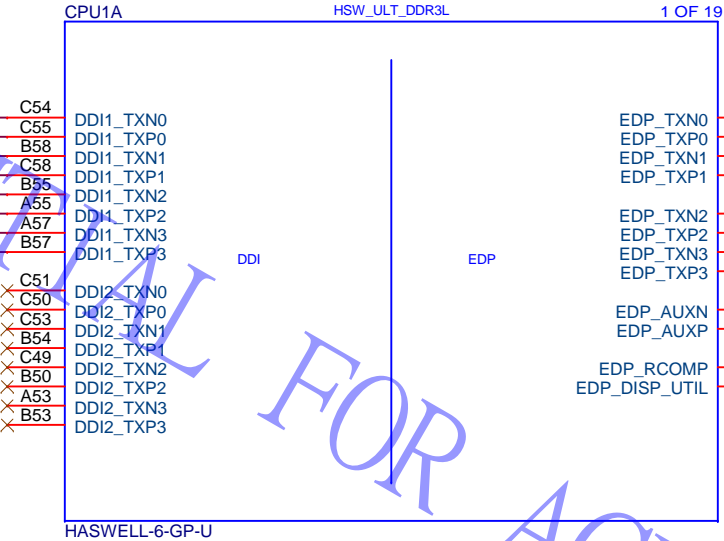
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SSID = CPU

HDMI

54 HDMI\_DATA\_CPU\_N2  
54 HDMI\_DATA\_CPU\_P2  
54 HDMI\_DATA\_CPU\_N1  
54 HDMI\_DATA\_CPU\_P1  
54 HDMI\_DATA\_CPU\_N0  
54 HDMI\_DATA\_CPU\_P0  
54 HDMI\_DATA\_CPU\_N3  
54 HDMI\_DATA\_CPU\_P3



EDP\_TXN0  
EDP\_TXP0  
EDP\_TXN1  
EDP\_TXP1  
  
EDP\_TXN2  
EDP\_TXP2  
EDP\_TXN3  
EDP\_TXP3  
  
EDP\_AUXN  
EDP\_AUXP  
  
EDP\_RCOMP  
EDP\_DISP\_UTIL

C45  
B46  
A47  
B47  
  
C47  
C46  
A49  
B49  
  
A45  
B45  
  
D20  
A43

eDP\_TX\_CPU\_N0 52  
eDP\_TX\_CPU\_P0 52  
eDP\_TX\_CPU\_N1 52  
eDP\_TX\_CPU\_P1 52  
  
eDP\_AUX\_CPU\_N 52  
eDP\_AUX\_CPU\_P 52

eDP



Layout Note:

Design Guideline:  
EDP\_COMP keep routing length max 100 mils.  
Trace Width:20 mils.

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω ±1%	Max = 100 mils

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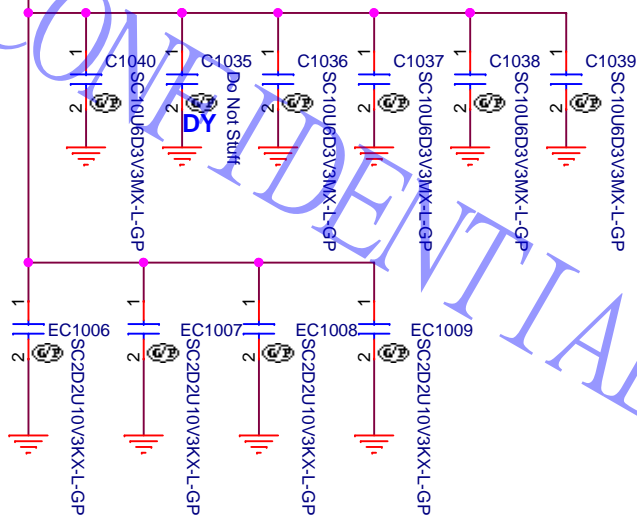
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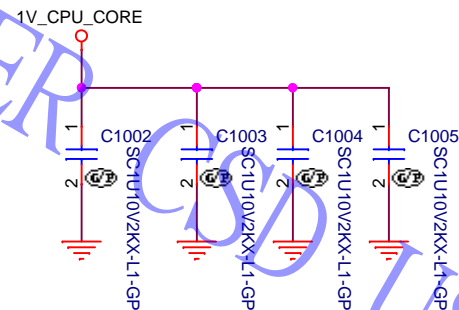
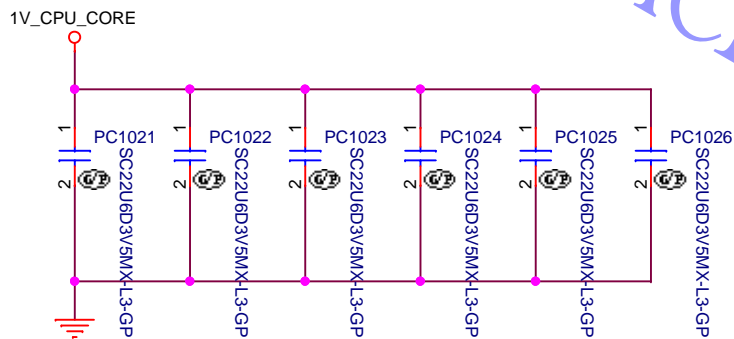
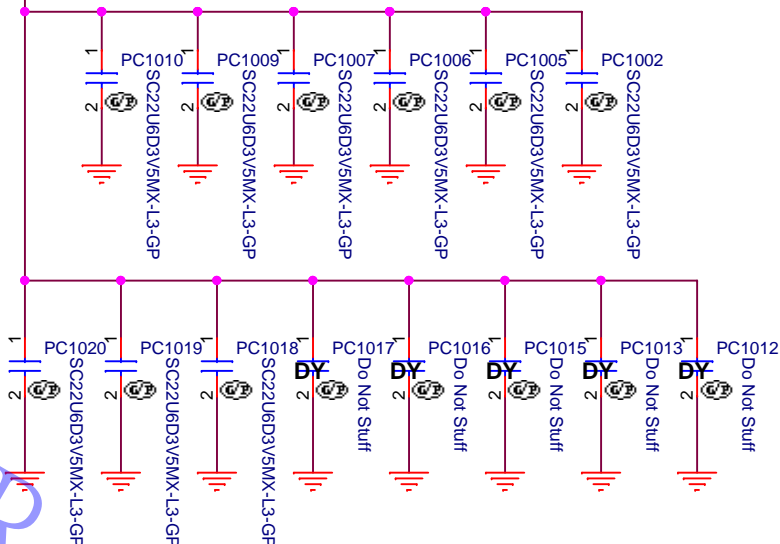
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1D35V\_S3  
**Power current=3A**



For Intel Recommend EE Part

1V\_CPU\_CORE  
**Power current=25A**



For Intel Recommend EE Part

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**CPU (Power CAP1)**

Size

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Document Number

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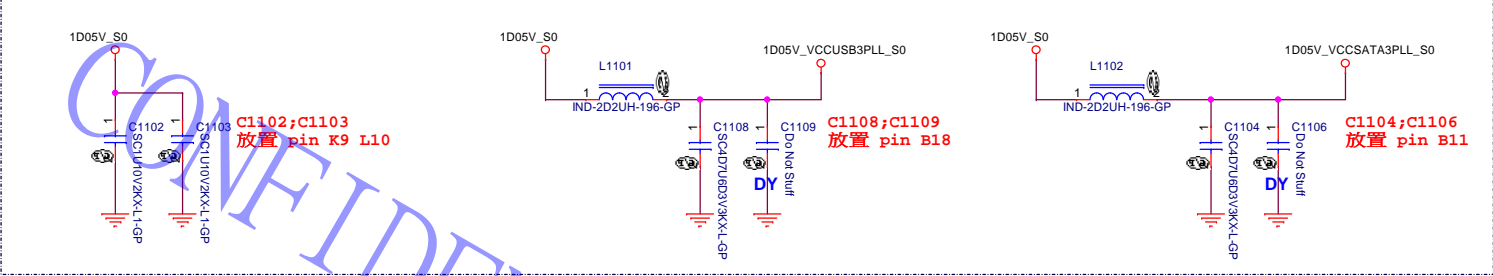
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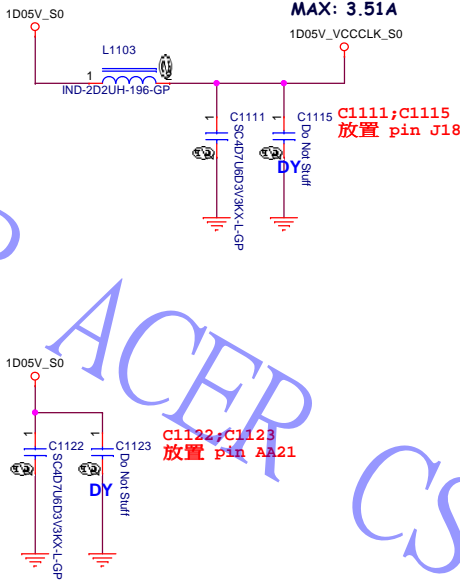
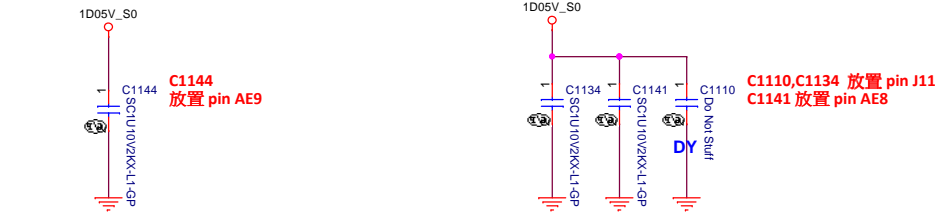
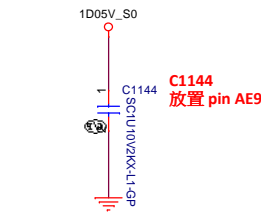
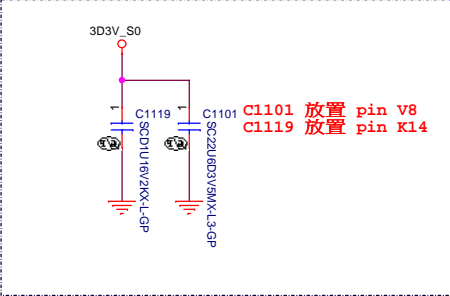
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擺放電容的位置請參考 Page 21,每個位置如下

MAX: 3.074A



MAX: 0.285A



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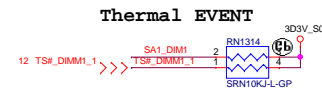


**SSID = MEMORY**

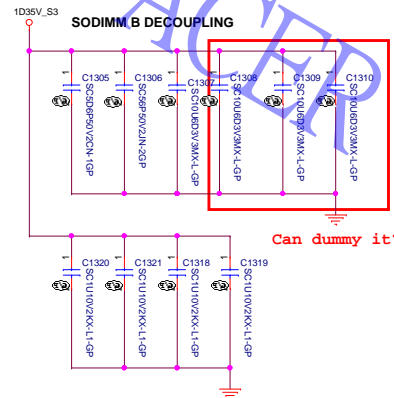


**Note:**  
SO-DIMMB SPD Address is 0xA4  
SO-DIMMB TS Address is 0x34

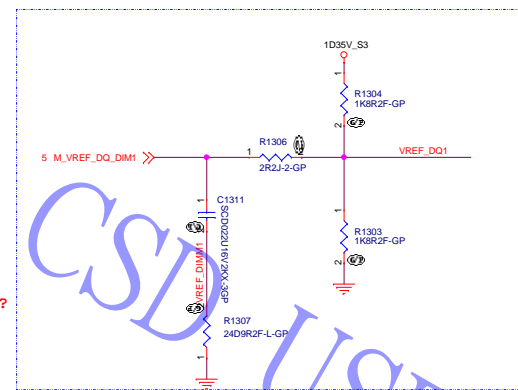
**SO-DIMMB is placed farther from the Processor than SO-DIMMA**



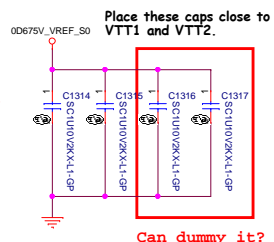
**Layout Note:**  
Place these Caps near  
SO-DIMMB.



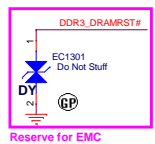
Can dummy it?



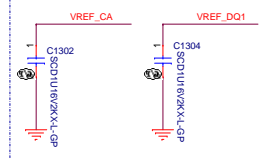
For Intel Recommend Close to DIMM



Can dummy it?



### Close RAM3 CA & DQ pin



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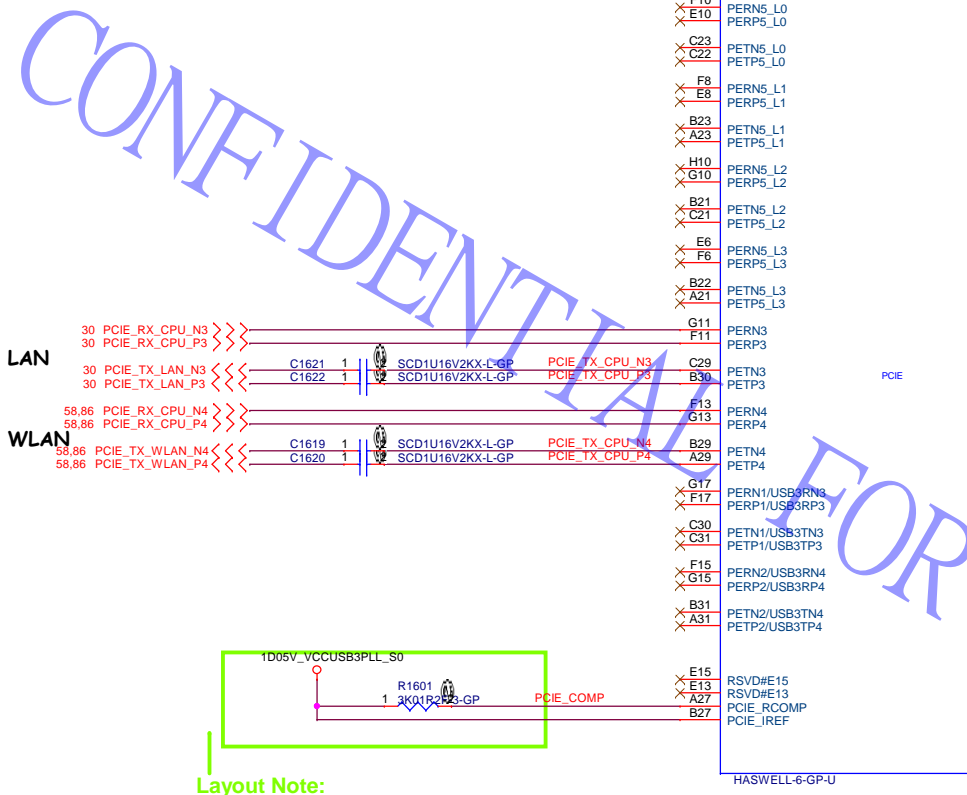
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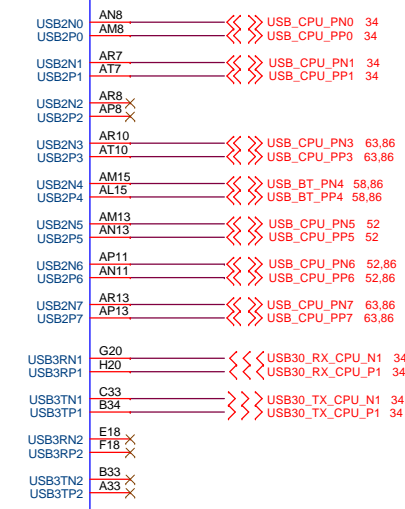
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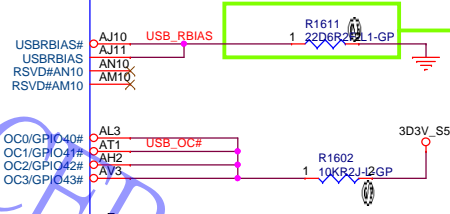
**Layout Note:**  
1. PCIE\_RCOMP/ PCIE\_IREF trace width=12-15mil  
2. Isolation Spacing: 12mil  
3. Total trace length<500mil

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
PCIE_RCOMP	4 mils min (breakout) 12-15 mils (trace) <b>Note:</b> Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	3k ohm ±1% pulled to VCCUSB3PLL.	Max total = 500 mils
PCIE_IREF	4 mils min (breakout) 12-15 mils (trace) <b>Note:</b> Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	No resistor. Must connect directly to VCCUSB3PLL.	Max total = 500 mils



**USB 3.0**  
**USB 2.0**  
**USB 2.0 IO**  
**BT**  
**TS**  
**CCD**  
**Card Reader**  
**USB 3.0 port0**

Pair	Device
0	USB 3.0
1	USB 2.0
2	
3	USB 2.0 IO
4	BT
5	TS
6	CCD
7	Card Reader



**Layout Note:**  
1. USB\_COMP using 50 ohm single-ended impedance  
2. Isolation Spacing :15mil  
3. Total trace length<500mil

**USBRBIAS/USBRBIAS# Connection Guidelines**

- Short the USBRBIAS and the USBRBIAS# pins at the package and then route on the top layer to one end of a 22.6 Ω ±1% resistor to ground (see Figure 15-2).
- Route signal using 50 ohm single-ended impedance and 500 mils (12.7-mm) max trace length and no longer than 450 mils to resistor.
- Avoid routing next to clock pins or under stitching capacitors. Recommended minimum spacing to other signal traces is 15 mils (0.381 mm).

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
PCIE_RCOMP	4 mils min (breakout) 12-15 mils (trace) <b>Note:</b> Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	3k ohm ±1% pulled to VCCUSB3PLL.	Max total = 500 mils
PCIE_IREF	4 mils min (breakout) 12-15 mils (trace) <b>Note:</b> Must maintain low DC resistance routing (<0.2 ohm).	At least 12 mils to any adjacent high speed I/O.	No resistor. Must connect directly to VCCUSB3PLL.	Max total = 500 mils

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CPU (PCI/USB)

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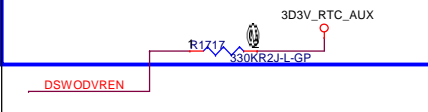
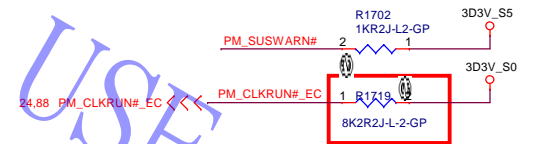
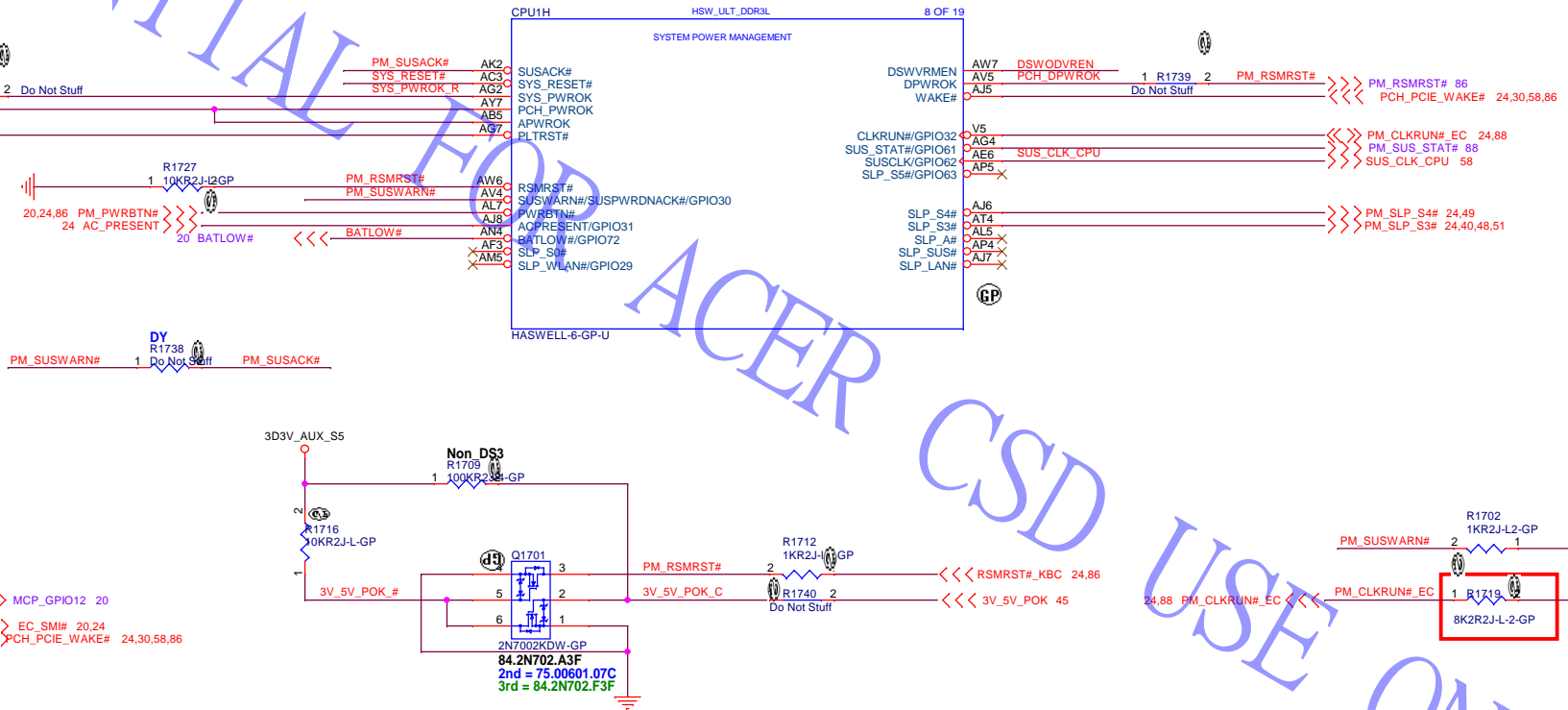
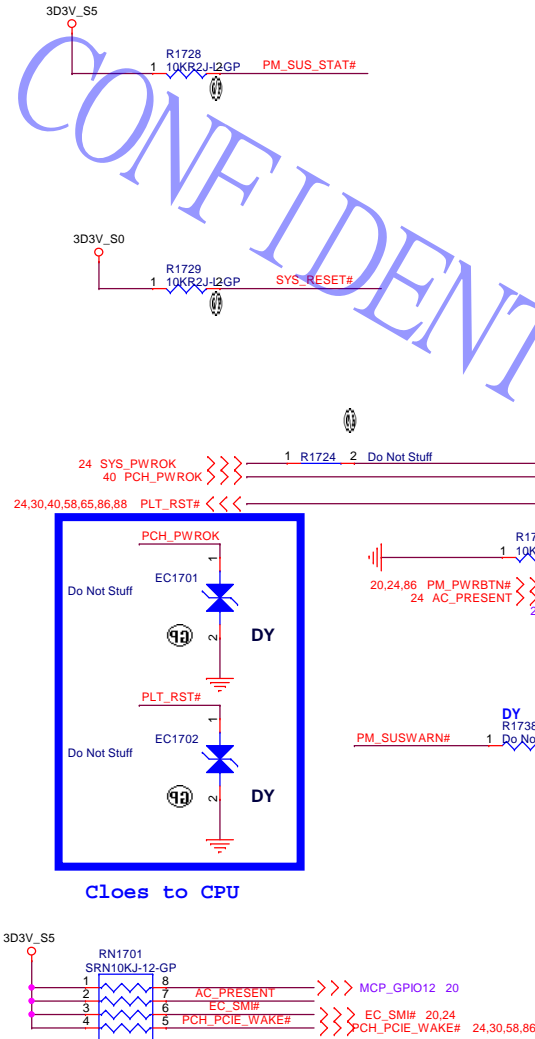
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Bit	Description
31:3	Reserved
2	<p><b>WAKE# Pin Deep Sx Enable (WAKE_PIN_DSX_EN)</b> - R/W. When this bit is '1', the PCI Express WAKE# pin is monitored while in Deep Sx, supporting wake from Deep Sx due to assertion of this pin. In this case the platform must externally pull-up the pin to the DSW (instead of pulling-up to the SUS as historically been the case).</p> <p>When this bit is '0':</p> <ul style="list-style-type: none"> <li>Deep Sx configurations: The PCH internal pull-down on the WAKE# pin is enabled in Deep Sx and during G3 exit and the pin is not monitored during this time.</li> <li>Deep Sx disabled configurations: The PCH internal pull-down on the WAKE# pin is never enabled.</li> </ul> <p><b>NOTE:</b> Deep Sx disabled configuration must leave this bit at '0'.</p>

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

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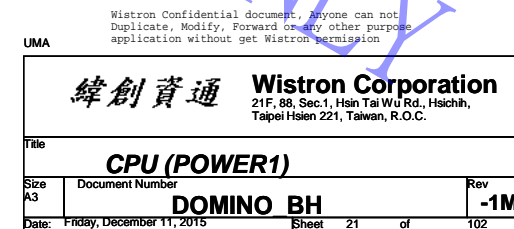
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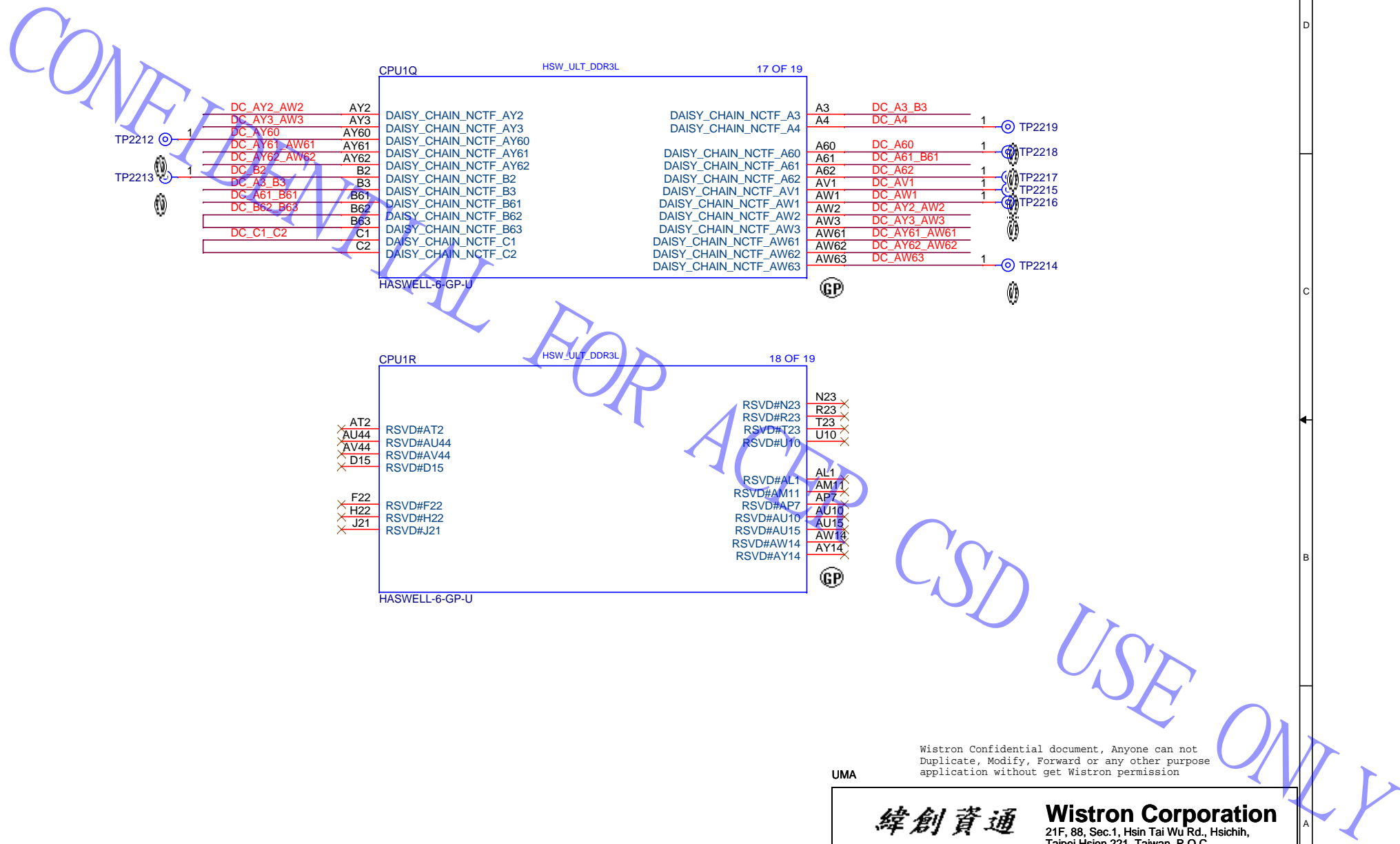






1. Required only on external SUS.
2. Placeholder only. Does not need to be stuffed.
3. The following pins are not to be connected and be left floating. Test point is optional on these pins: AC20, Y20, K18, M20, V21.
4. Note that some decoupling capacitors are shared between more than 1 rail. Follow the "Place capacitors near balls" instructions above to ensure this sharing is optimized.
5. Capacitors should be placed less than 100 mils (2.54 mm) from the edge of package.
6. For description of (R)unway, and (E)dge decoupling capacitor placement, please refer to [Section 41.3, "Loop Inductance Reduction Decoupling"](#) on page 532.





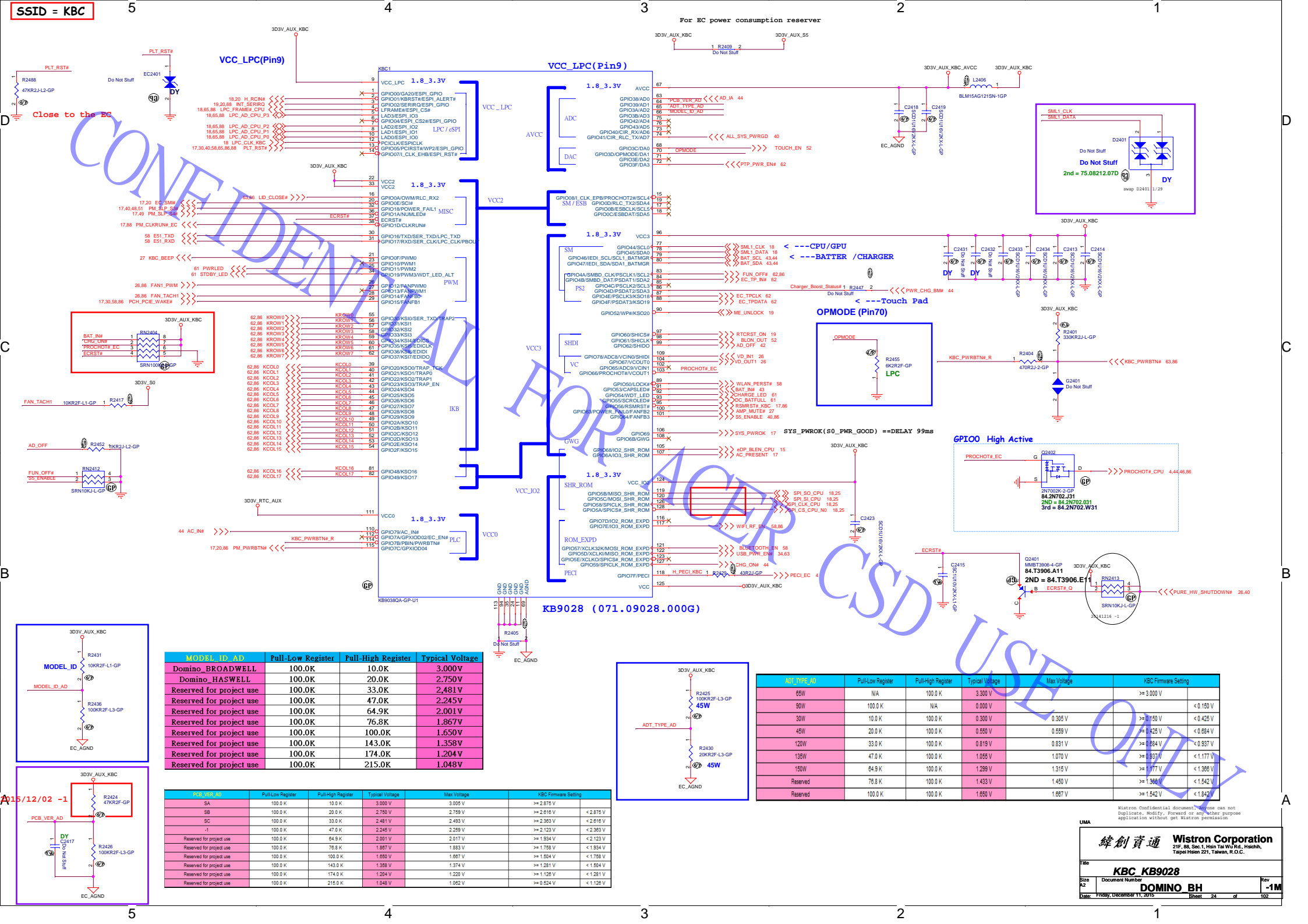
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CPU (RSVD)			
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**SPI FLASH ROM (8M byte) for PCH**

*SPI ROM Equal length need to less than 500mil*

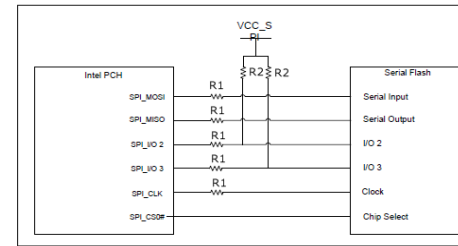
SPI FLASH ROM (8M byte)

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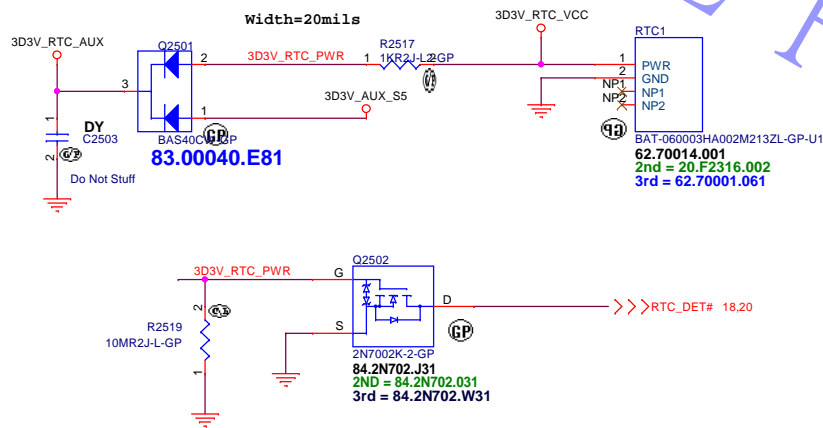
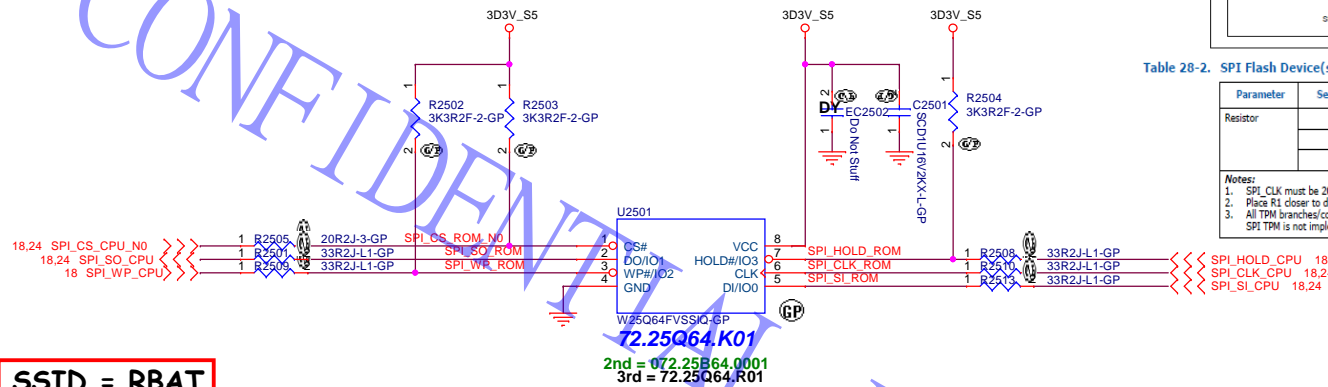
2ND=072.25B64.0001(Gigadevice GD25B64BSIGR)

purge=72.25Q64.K01 (WINBOND W25Q64FVSSIQ)

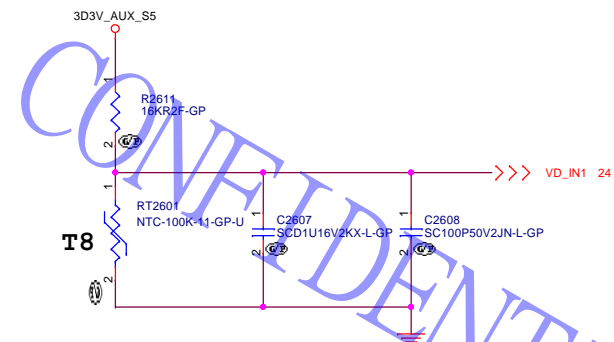
72.25647.00A (MXIC MX25L6473EM2I)



Parameter	Segment	Stackup	Unit	Routing Recommendation
Resistor	R1		ohm	15
	R2		ohm	1k
	R3		ohm	33

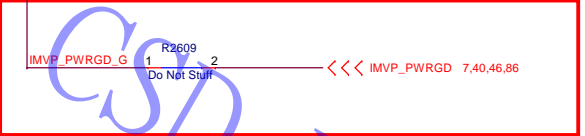
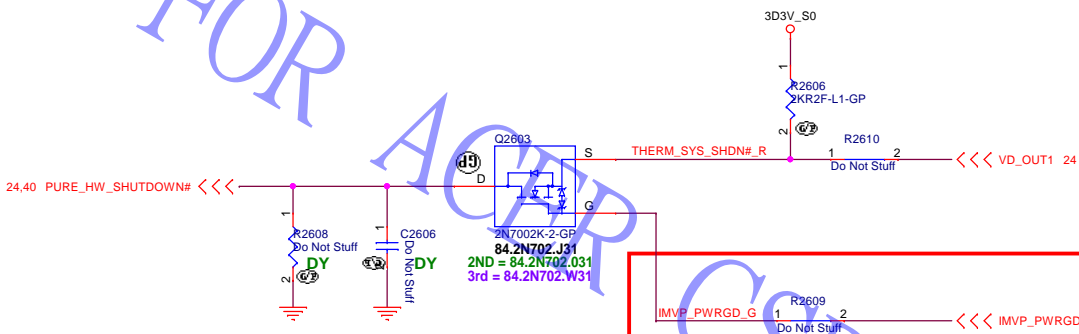
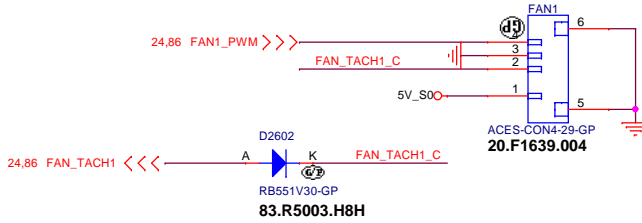
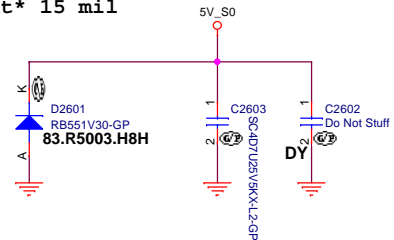


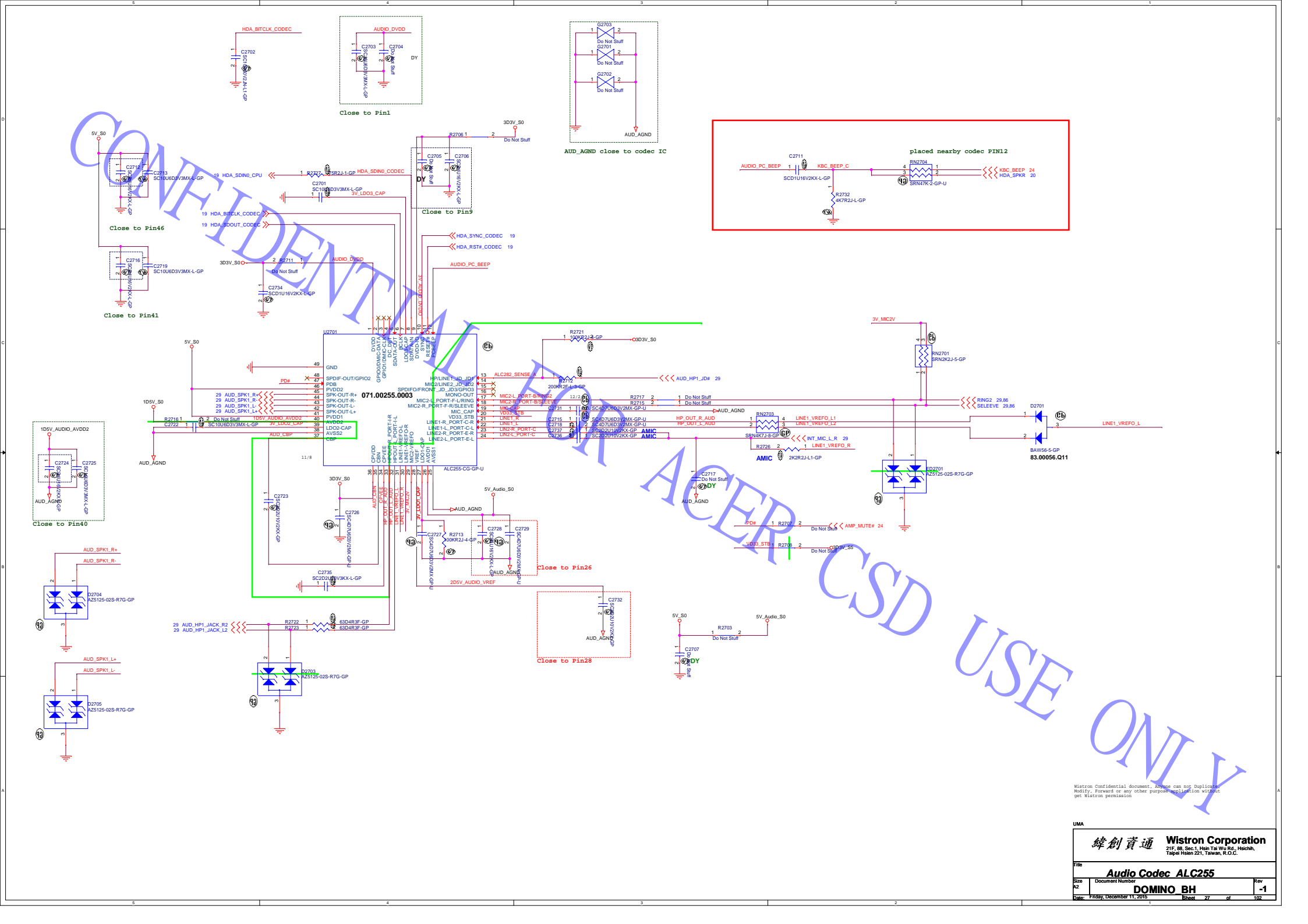
SSID = Thermal



RT2601 close CPU and Vcore chock

\*Layout\* 15 mil





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Size  
A4

Document Number

**Domino**

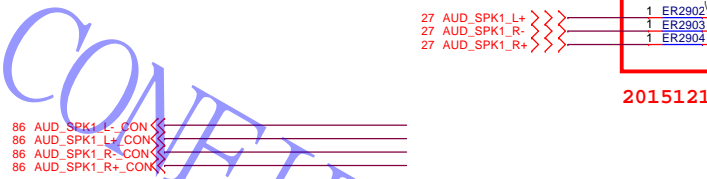
Rev  
**-1**

Date: Friday, December 11, 2015

Sheet 28 of 102

SSID = AUDIO

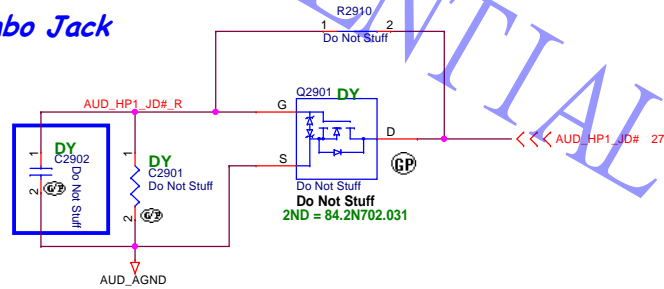
Speaker



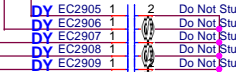
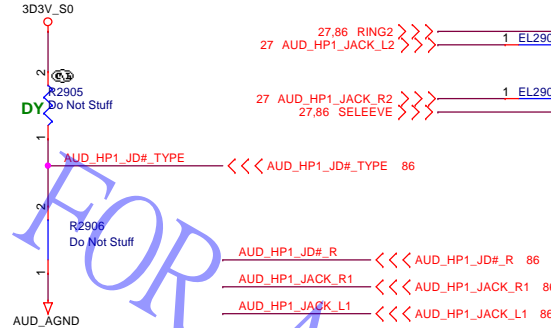
20151210 -1

Layout Note:  
Trace width=40mil 20151208 -1

Combo Jack

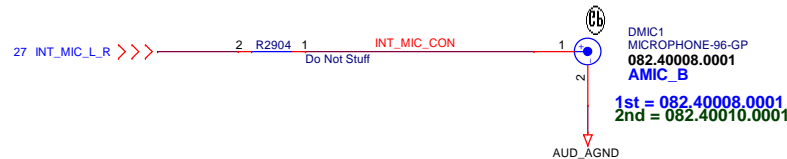


2ND = 84.2N702.031



AUDIO-JK492-GP  
022.10002.0811  
2nd = 022.10002.0901

DMIC AMIC



DMIC1 MICROPHONE-96-GP  
082.40008.0001  
AMIC\_B  
1st = 082.40008.0001  
2nd = 082.40010.0001

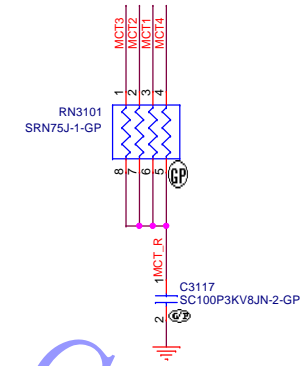
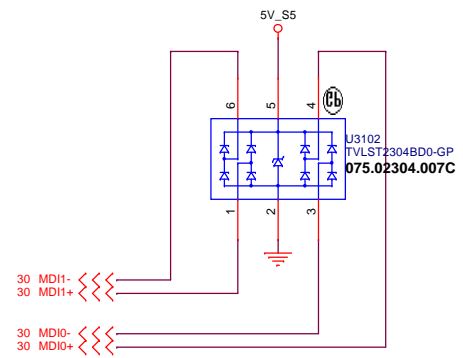
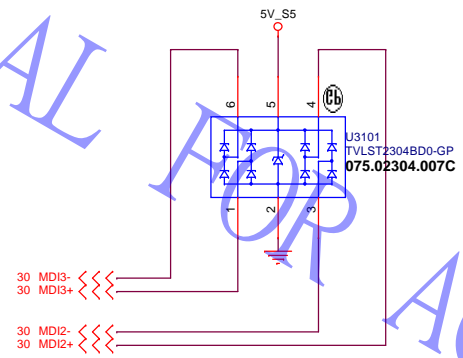
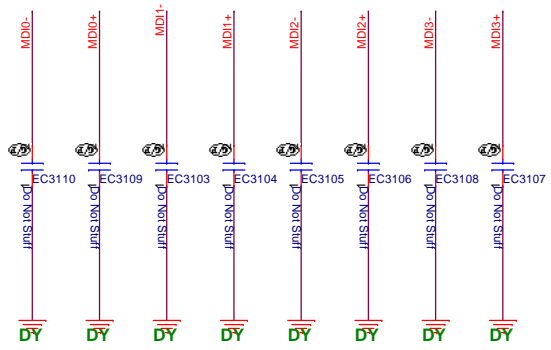
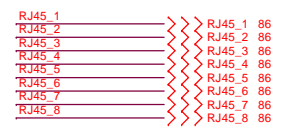
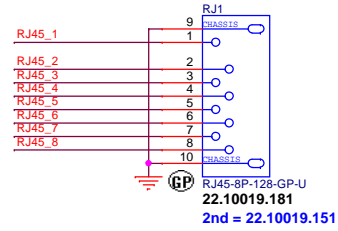
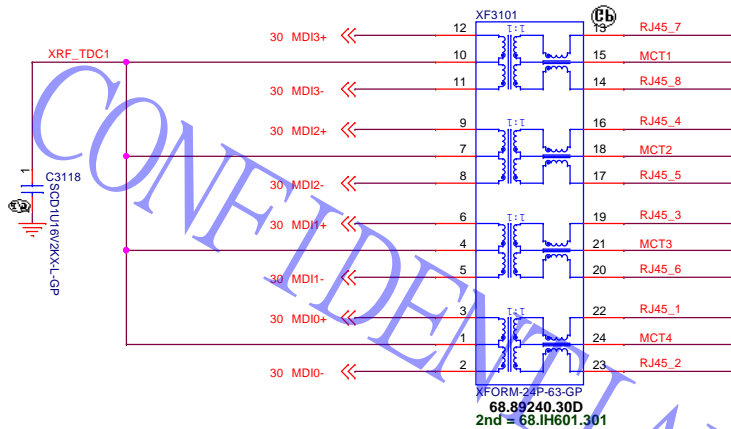
AMIC on board: mount DMIC1, R2904, DY AMIC1, R2901, R2902, R2903, EC2910, EC2911  
AMIC for cable: mount AMIC1, R2901, R2902, DY R2903, EC2910, EC2911, DMIC1, R2904  
DMIC for cable: mount AMIC1, R2903, DY R2901, R2902, EC2910, EC2911, DMIC1, R2904

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Audio Jack	
Size	Document Number
Custom	DOMINO BH
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SSID = LAN



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***RTS5170(CARD READER)***

Size  
A4

Document Number

**DOMINO BH**

Rev  
**-1**

Date: Friday, December 11, 2015

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SSID = SDIO

# SD//MS Card Reader

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Title

**CARD Reader CONN**

Size  
Custom

Document Number

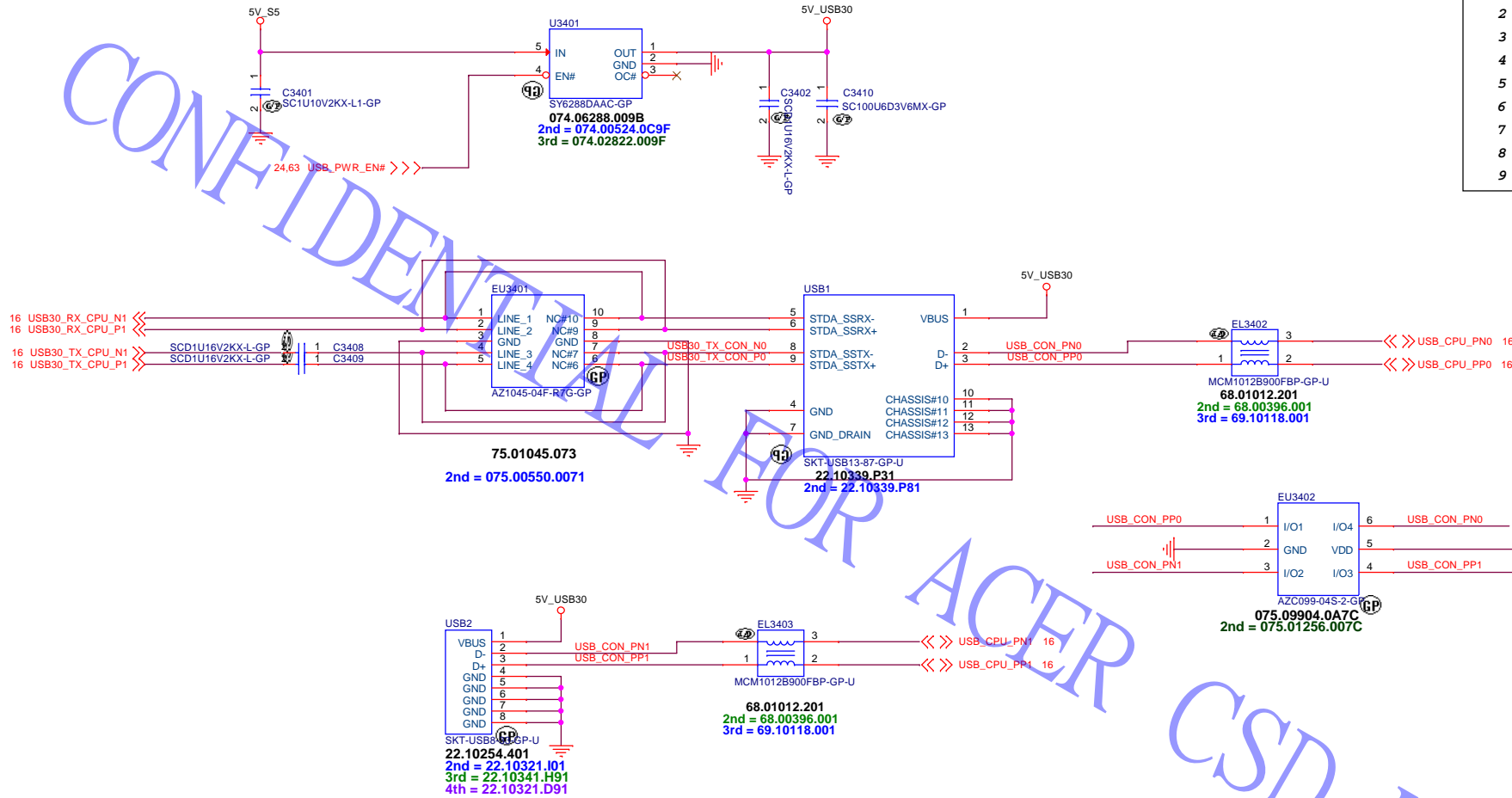
**DOMINO BH**

Rev  
**-1**

Date: Friday, December 11, 2015

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# Low Active 2A



## USB 3.0 Connector Pin definition

1	POWER	
2	USB 2.0 D-	
3	USB 2.0 D+	
4	GND	
5	StdA_SSRX-	SuperSpeed RX
6	StdA_SSRX+	
7	GND	
8	StdA_SSTX-	SuperSpeed TX
9	StdA_SSTX+	

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Title		
USB 2.0 / 3.0 Port		
Size	Document Number	Rev
A3	DOMINO BH	-1
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Title			
USB HUB			
Size	Document Number		Rev
Custom	DOMINO BH		-1
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Title

**USB Charger**

Size  
A4

Document Number

**DOMINO BH**

Rev  
**-1M**

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Title <b>PCIE to USB</b>			
Size B	Document Number <b>DOMINO BH</b>		Rev <b>-1M</b>
Date: Friday, December 11, 2015		Sheet 37	of 102

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Title			
USB Redriver			
Size	Document Number	Rev	
A3	DOMINO BH	-1M	
Date: Friday, December 11, 2015		Sheet	38 of 102

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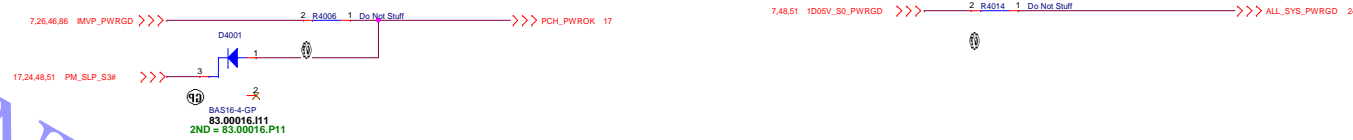
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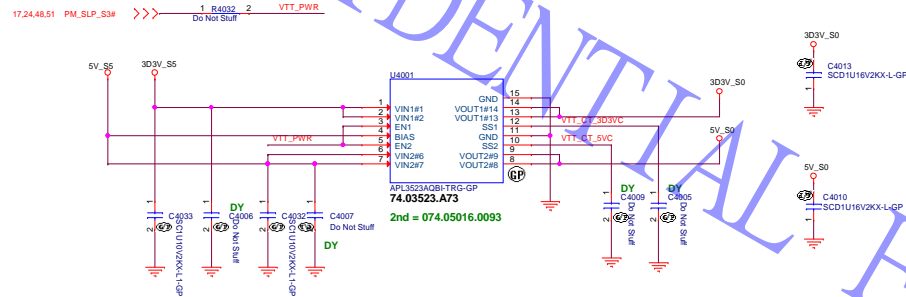
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Title			
DS3			
Size	Document Number		Rev
A4	DOMINO BH		-1M
Date: Friday, December 11, 2015		Sheet 39 of	102

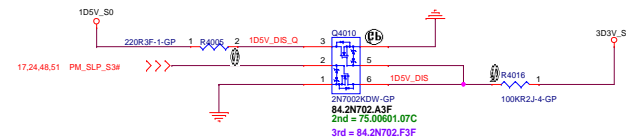
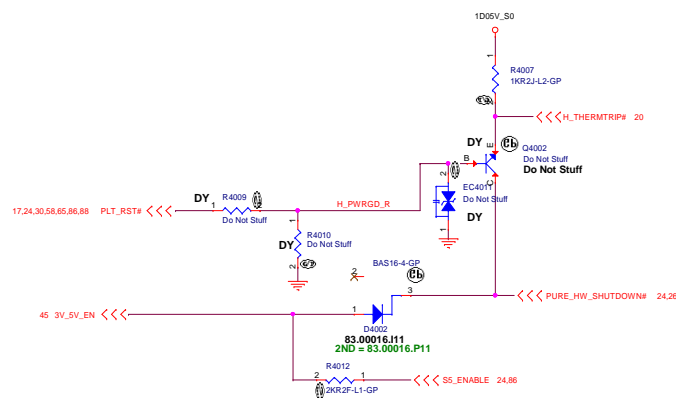
### *Power Sequence*



## ANNIE Run Power



### *Discharge circuit*





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Title

**(Reserved)**

Size  
A4

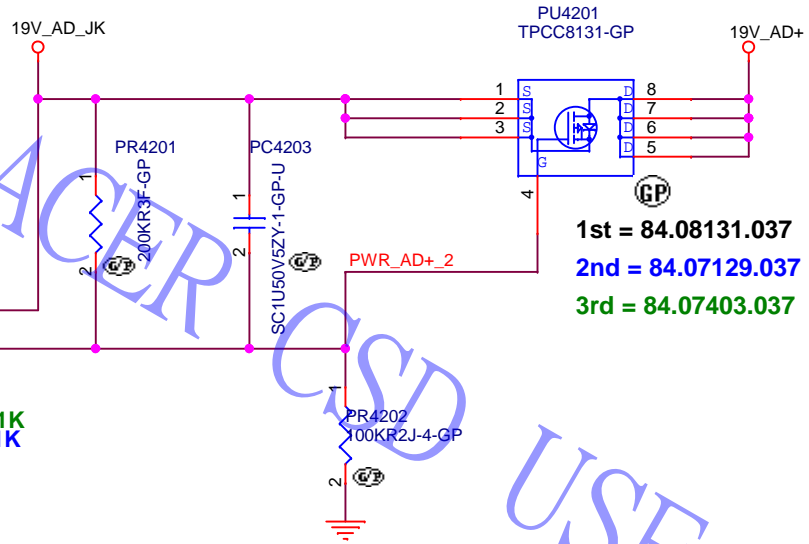
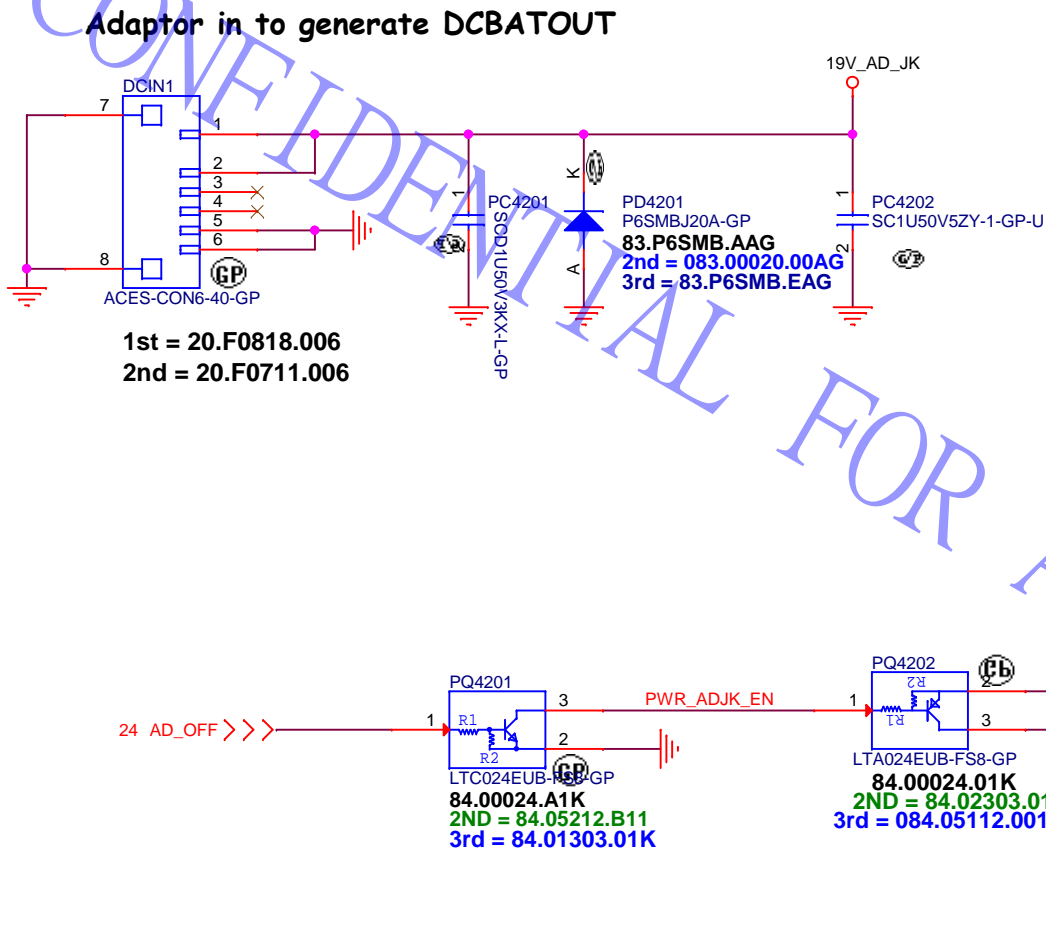
Document Number

**DOMINO BH**

Rev  
**-1M**

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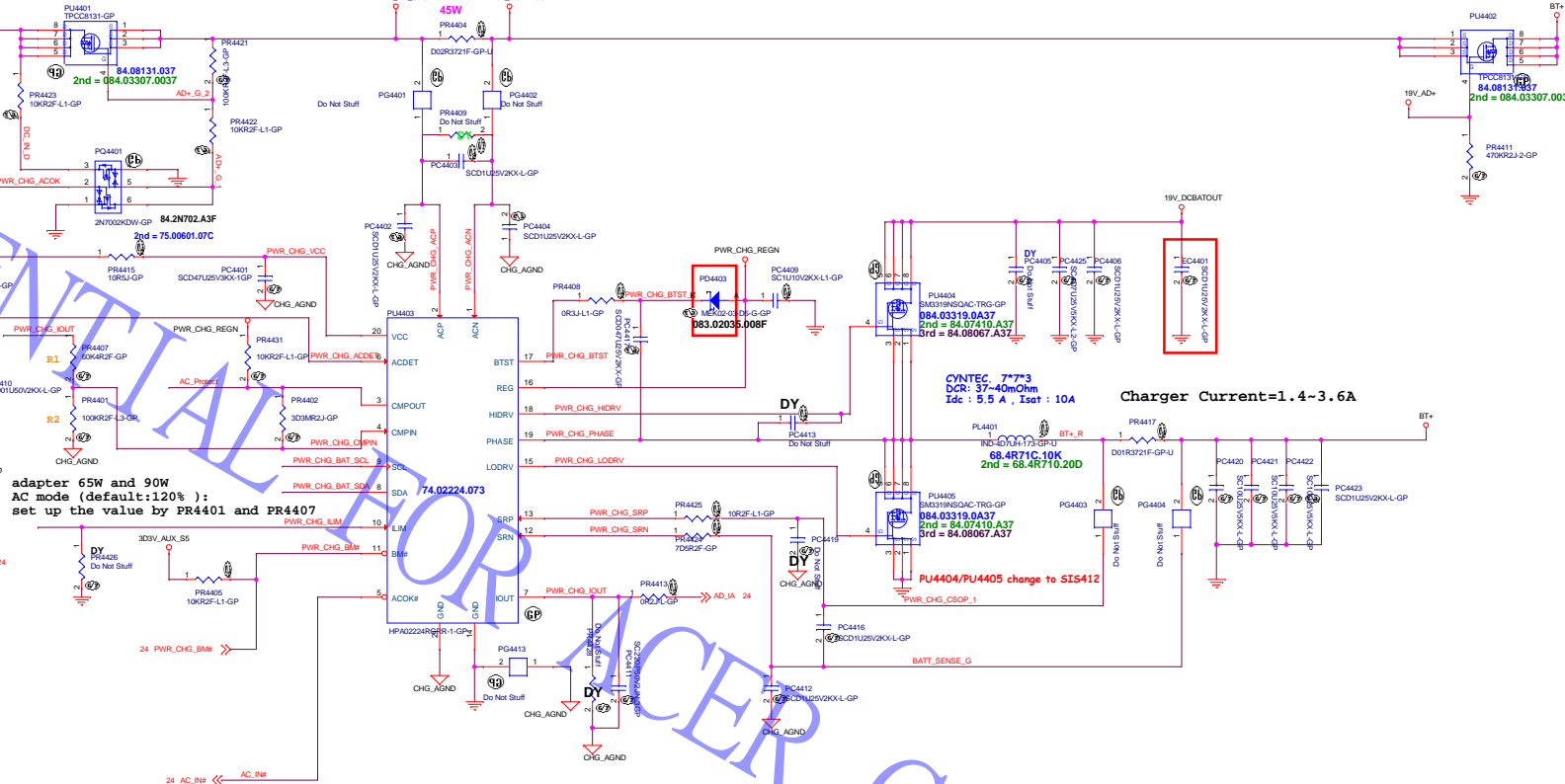
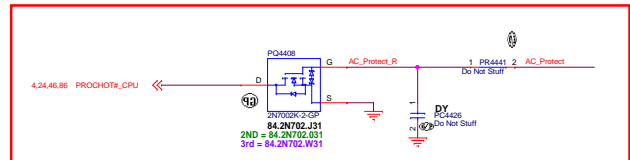
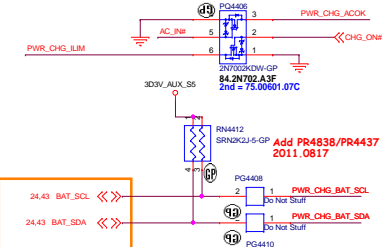
# SSID = Charger

3rd	7th	10th	13th	16th	19th	22nd	25th	28th	31st	34th	37th	40th	43rd	46th	49th	52nd	55th	58th	61st	64th	67th	70th	73rd	76th	79th	82nd	85th	88th	91st	94th	97th	100th
45W	AC+Sense	High	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01
90W	AC+Sense	High	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.02
135W	AC+Sense	High	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03	0.03

45W	90W
PR4404	20m(64.80205.7FF)
PR4407	60.4K(64.60425.6DL)
PR4401	100K(64.10035.13L)

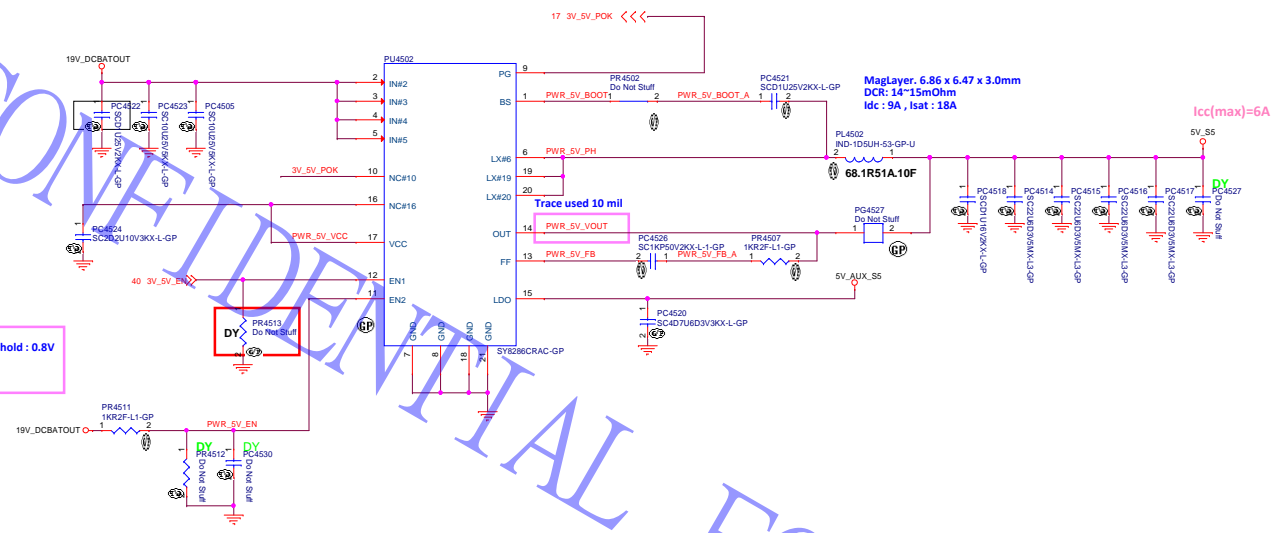


adapter 65W and 90W  
AC mode (default:120%)  
set up the value by PR4401 and PR4407

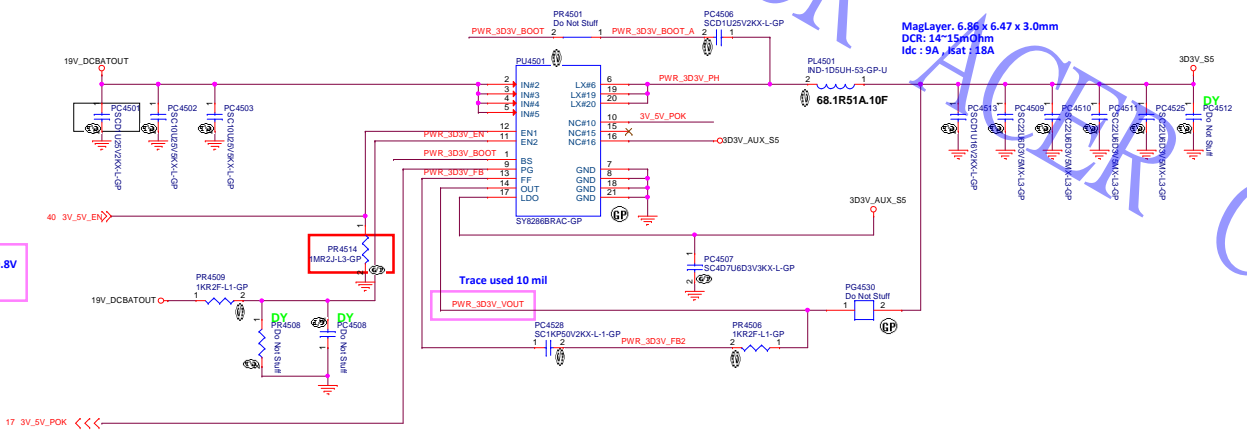


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EN rating 25V  
EN Rising Threshold : 0.8V  
Ilimit : 8A



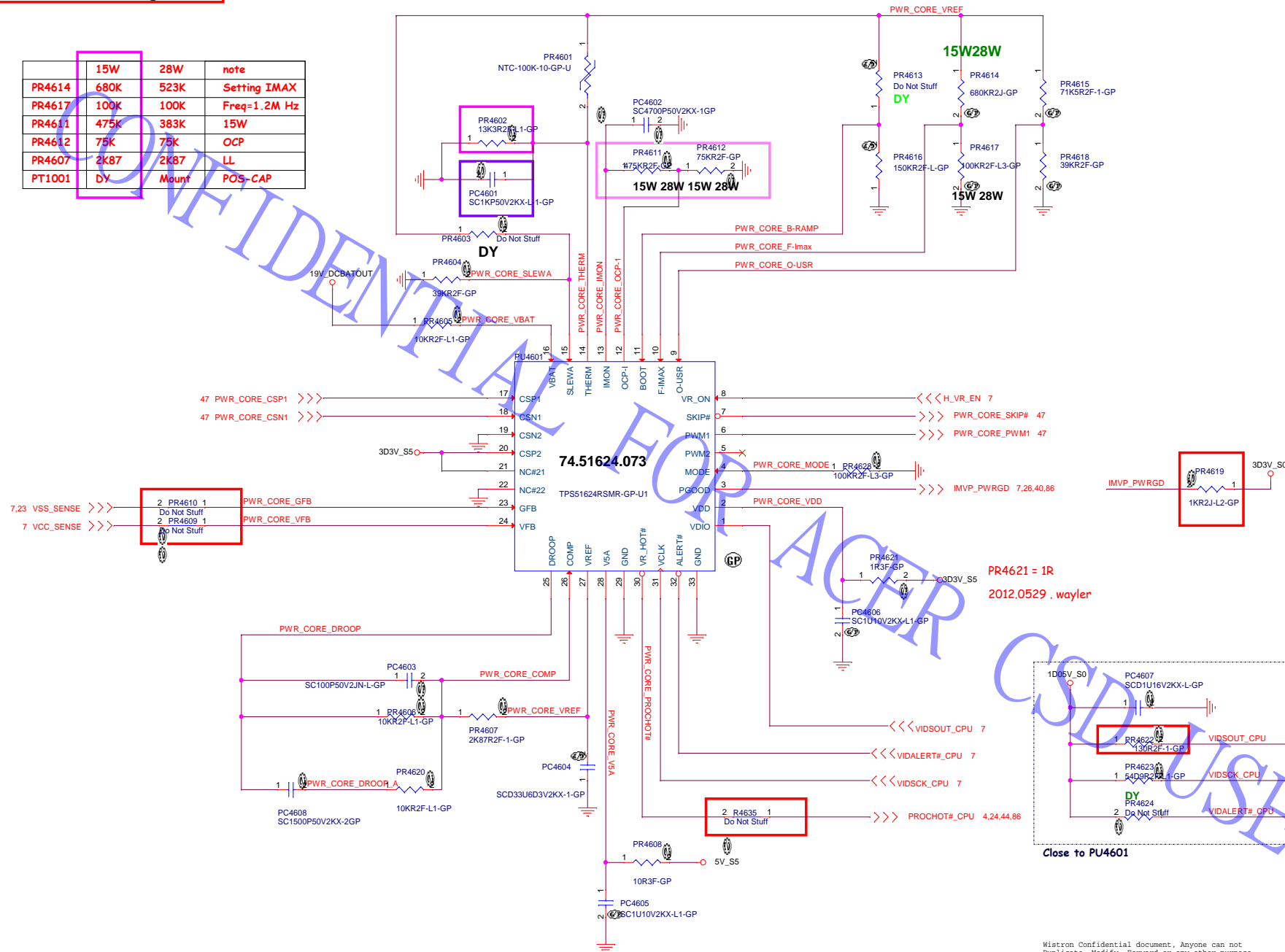
EN rating 25V  
EN Rising Threshold : 0.8V  
Ilimit : 8A



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**SSID = CPU.Regulator**

	15W	28W	note
PR4614	680K	523K	Setting IMAX
PR4617	100K	100K	Freq=1.2M Hz
PR4611	475K	383K	15W
PR4612	75K	75K	OCF
PR4607	2K87	2K87	LL
PT1001	DY	Mount	POS-CAP



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**TPS51624 CPUCORE(1/2)**

Size

Document Number

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Rev
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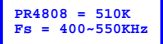
Sheet 46

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17,24,40,51 PM\_SLP\_S3# >>>

7,40,51 1D05V\_S0\_PWRGD <<



STATE	S3	S5	VDDQ	VTTREF	VTT
S0	H	H	1	1	1
S3	L	H	1	1	0 (high-Z)
S4/5	L	L	0 (discharge)	0 (discharge)	0 (discharge)



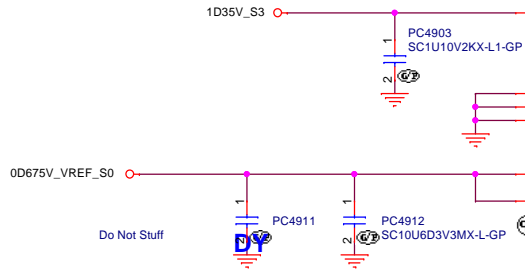
# VDDQ ENABLE CONTROL

17,24 PM\_SLP\_S4#  
12 DDR\_PG\_OUT

PR5108 = 510K  
Fs = 400-550KHz

2015/12/02 -1

12 DDR\_PG\_OUT  
19V\_DCBATOUT  
17,24 PM\_SLP\_S4#  
12 DDR\_PG\_OUT



MAG: 7 x 7 x 3.0 mm  
DCR: 9m~10mOhm  
Idc: 10 A, Isat: 22A

TDC : 8A

IND-1UH-94-GP-U  
68.1R01B.10K

$$V_{out} = 0.75 \times (1 + R1/R2) \\ = 0.75 \times (1 + 8.06/10) \\ = 1.354V$$

Table1. The Truth Table of S3 and S5 pins

STATE	S3	S5	VDDQ	VTTREF	VTT
S0	H	H	1	1	1
S3	L	H	1	1	0 (high-Z)
S4/5	L	L	0 (discharge)	0 (discharge)	0 (discharge)

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Title TPS51716(1.35V\_S3/0.675V\_S0)

Size A3 Document Number DOMINO BH Rev -1  
Date: Friday, December 11, 2015 Sheet 49 of 102

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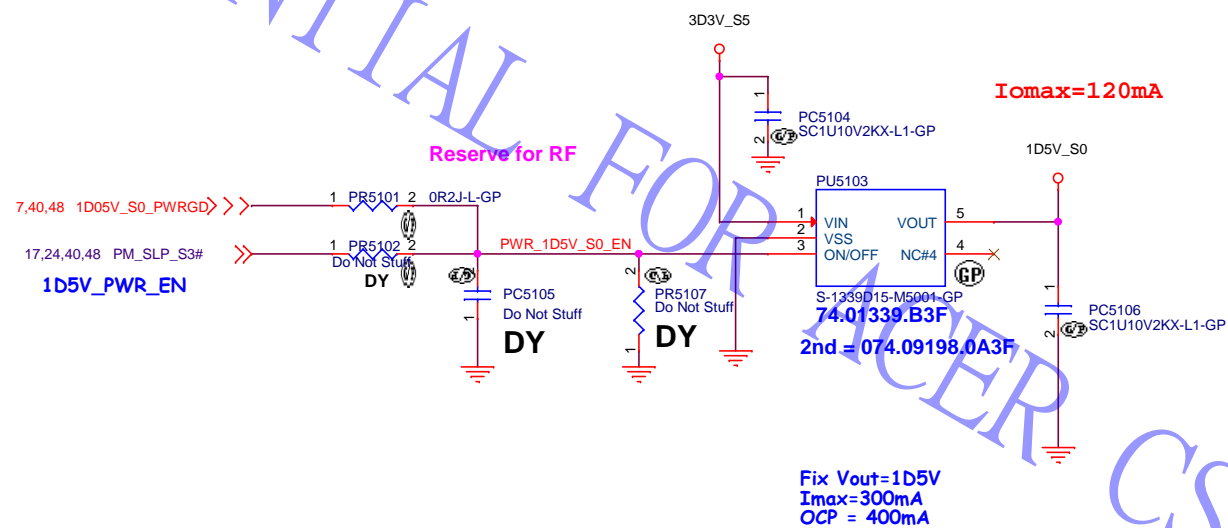
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Size A4	Document Number <b>DOMINO BH</b>		Rev <b>-1M</b>
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TLV70215 for 1D5V\_S0  
Enable=1.5V  
Disable=0.4V



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Title

**1D5V\_S0 SYW232**

Size  
Custom

Document Number

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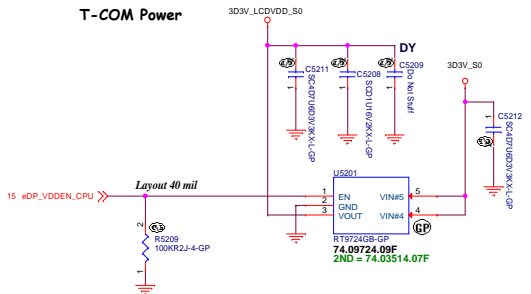
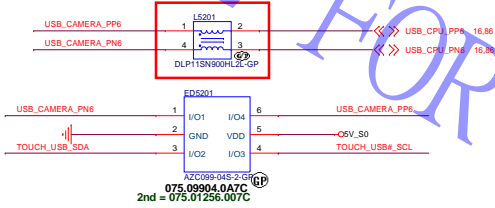
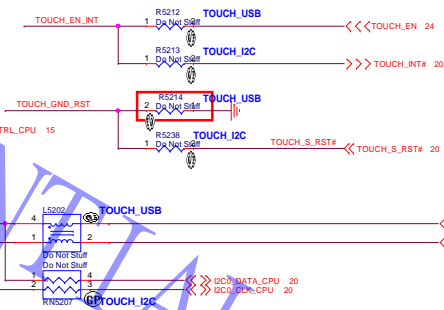
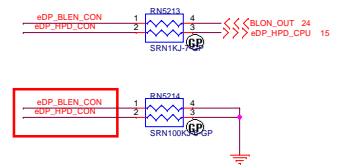
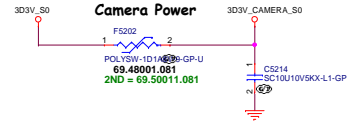
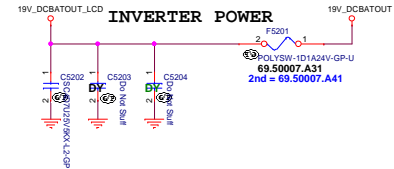
Rev

**-1M**

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DP_AUXP_LVDS_DATA	↔	DP_AUXP_LVDS_DATA	86
DP_AUXN_LVDS_CLK	↔	DP_AUXN_LVDS_CLK	86
DP_TXP0_LVDSA_D0_R	↔	DP_TXP0_LVDSA_D0_R	86
DP_TXN0_LVDSA_DQ_R#	↔	DP_TXN0_LVDSA_DQ_R#	86
DP_TXP1_LVDSA_D1_R	↔	DP_TXP1_LVDSA_D1_R	86
DP_TXN1_LVDSA_D1_R#	↔	DP_TXN1_LVDSA_D1_R#	86



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Title			
LCD Connector			
Size A2	Document Number	Rev	
DOMINO BH		-1	
Date:	Friday, December 11, 2015	Sheet 52 of	102

# Blanking

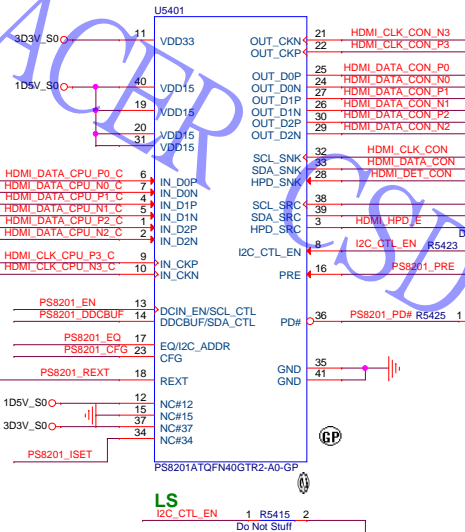
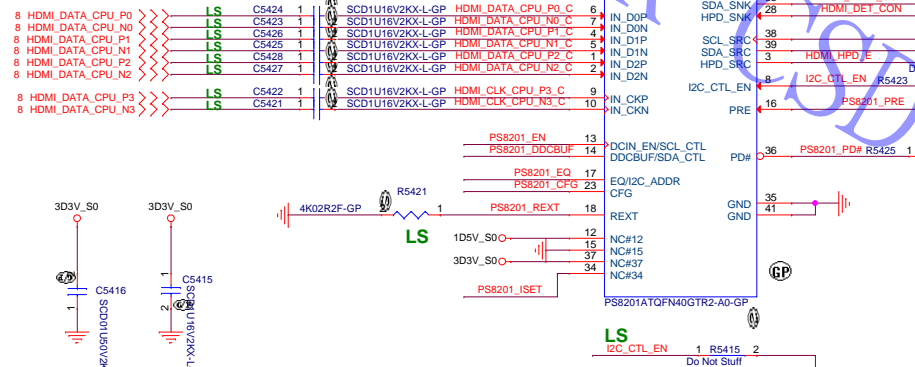
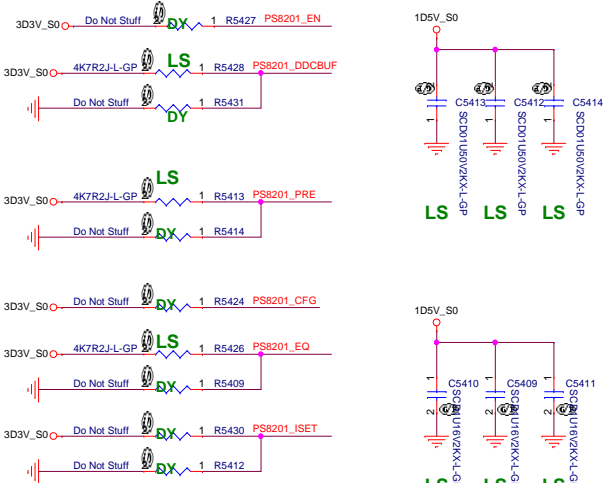
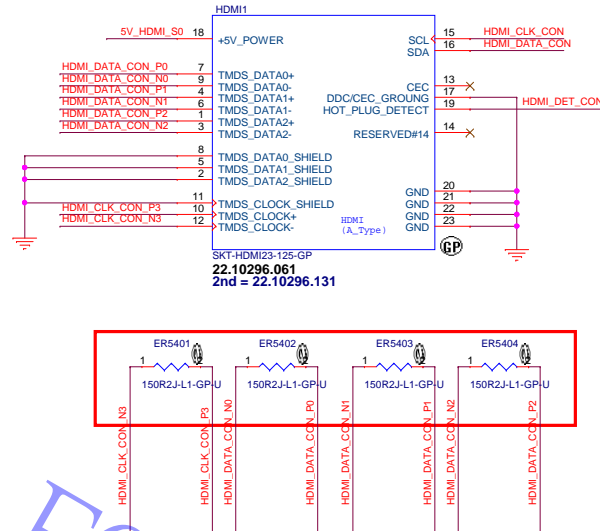
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Title		
CRT Connector		
Size	Document Number	Rev
A4	DOMINO BH	-1
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## HDMI Level Shifter & CONNECTOR

## HDMI1



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Size  
A4

Document Number

**DOMINO BH**

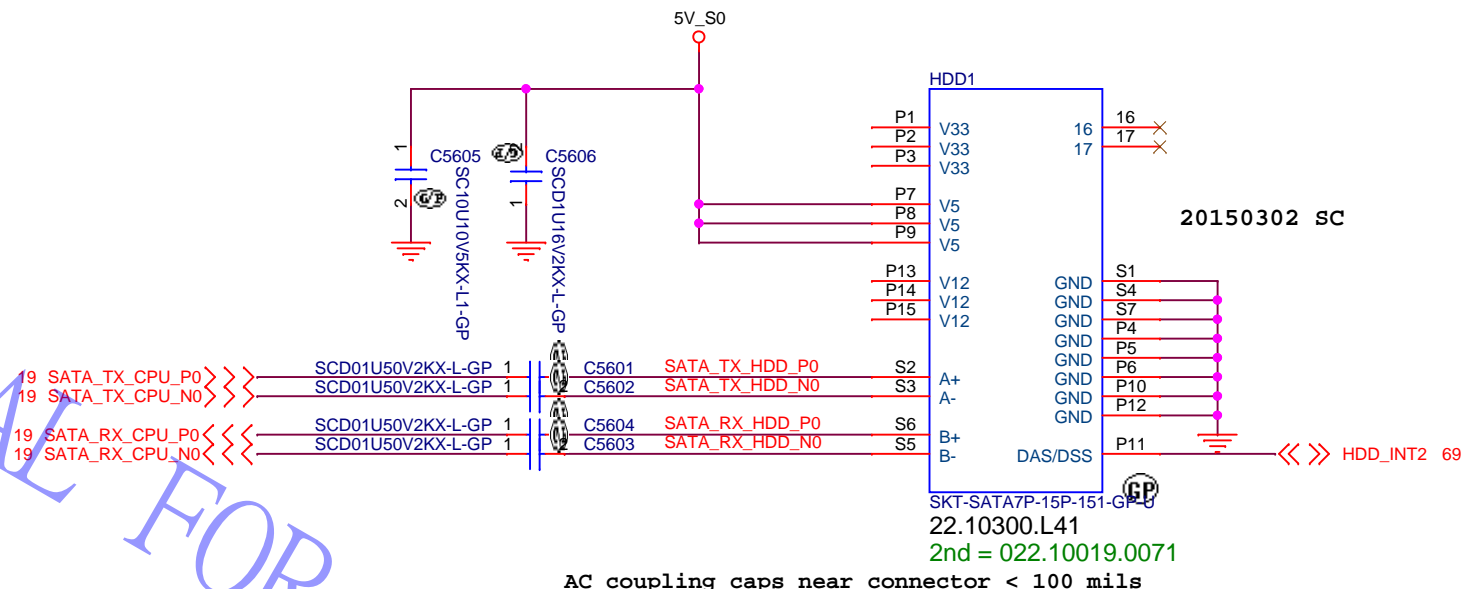
Rev  
**-1**

Date: Friday, December 11, 2015

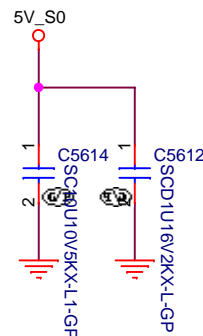
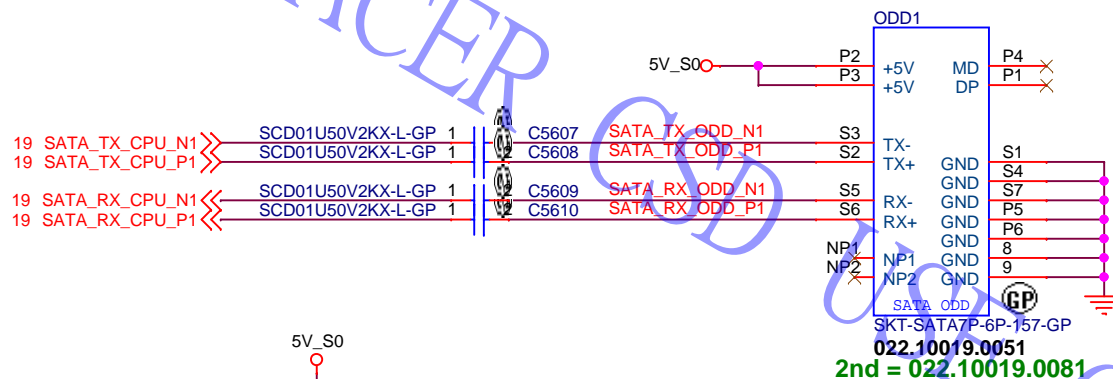
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SSID = SATA

# SATA HDD Connector



# ODD Connector



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Title

HDD / ODD / NGFF SSD

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AC coupling caps near connector < 100 mils



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Title

***Reserved***

Size  
A4

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**SSID = Wireless** *Mini Card Connector(802.11a/b/g/n)*



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Title			
<b>Mini card-WLAN</b>			
Size A3	Document Number		Rev
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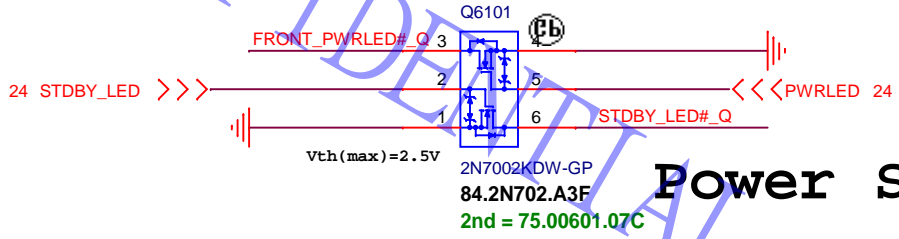
Title

Reserved

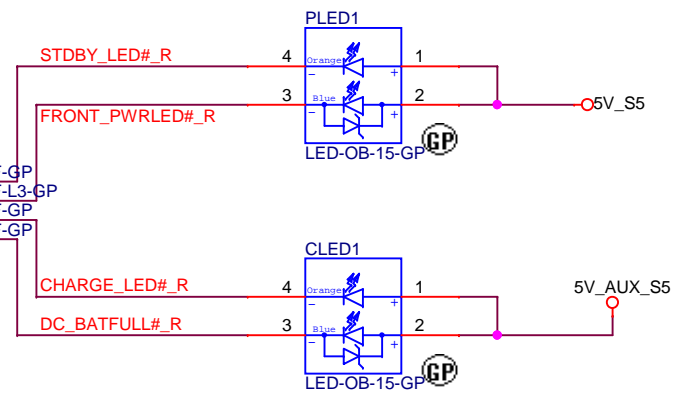
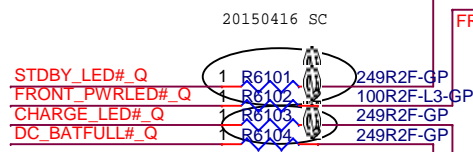
Size A4	Document Number <b>DOMINO BH</b>	Rev <b>-1</b>
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SSID = User.Interface

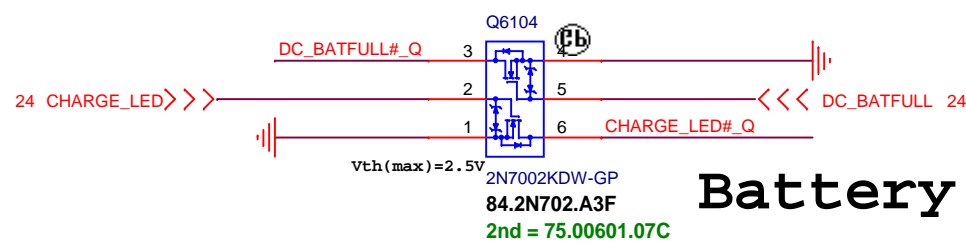
# Power button LED



# Power STDBY\_LED



# Battery LED2 (DC\_BATFULL)



# Battery LED1 (CHARGE)

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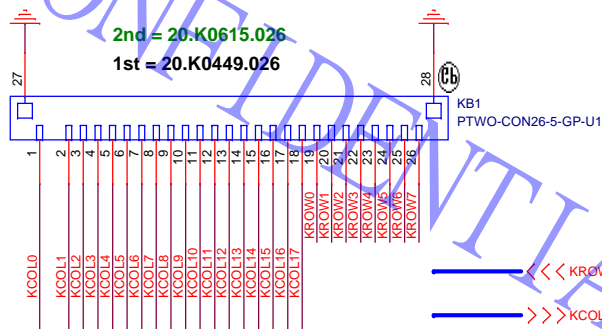
UMA		
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>LED Bard/Power Button</b>		
Size A4	Document Number <b>DOMINO BH</b>	Rev <b>-1</b>
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SSID = KBC

## Internal KeyBoard Connector

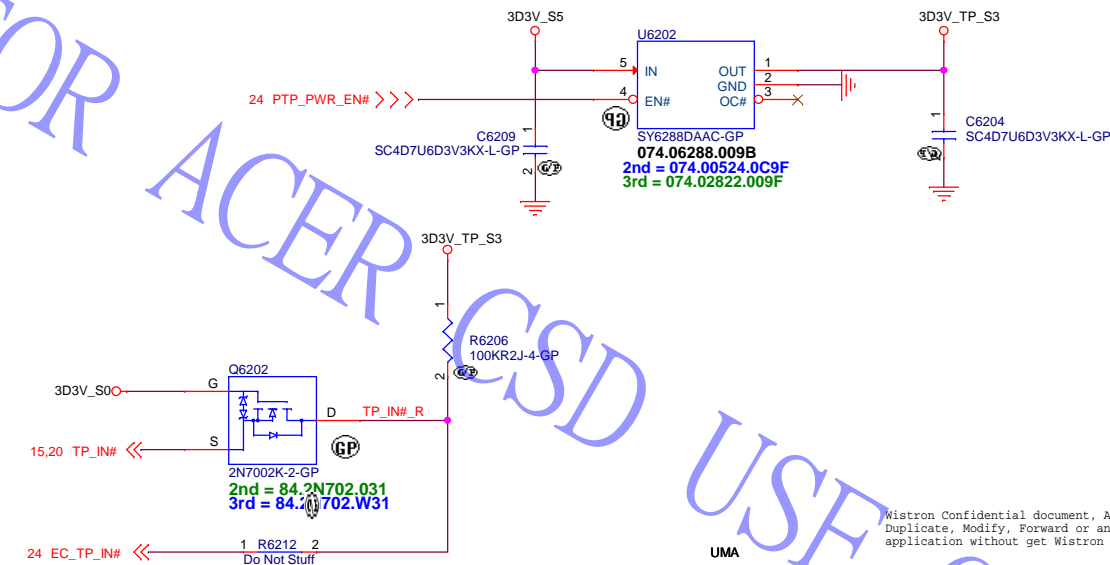
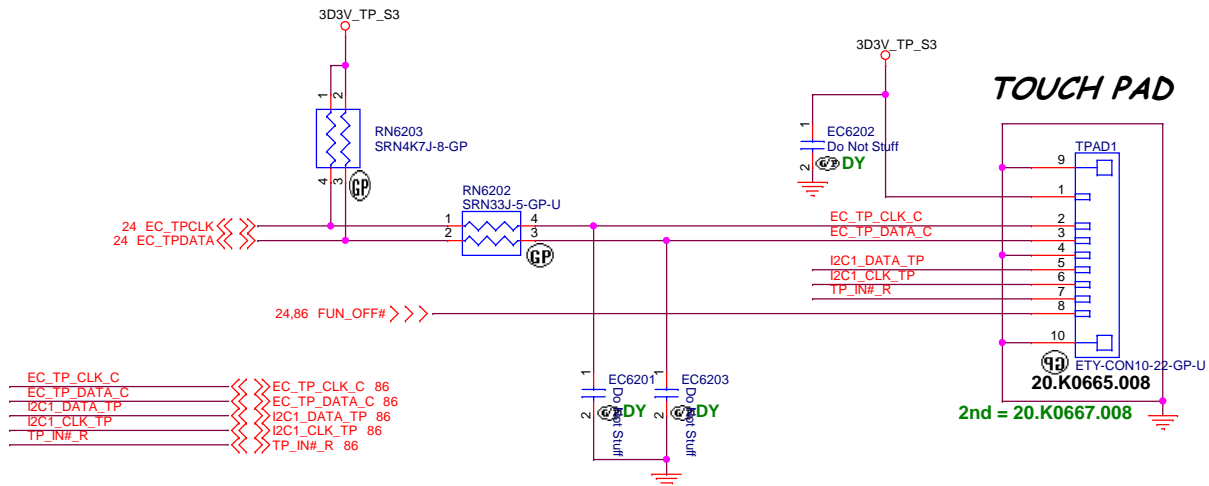
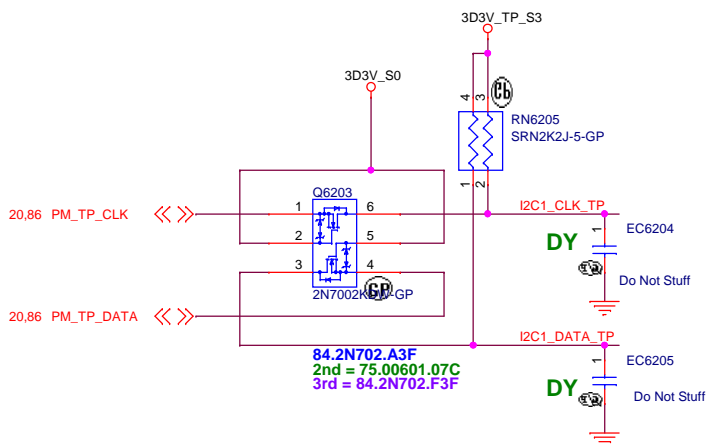
2nd = 20.K0615.026

1st = 20.K0449.026



MB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1  
KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26

26 **K/B** 1



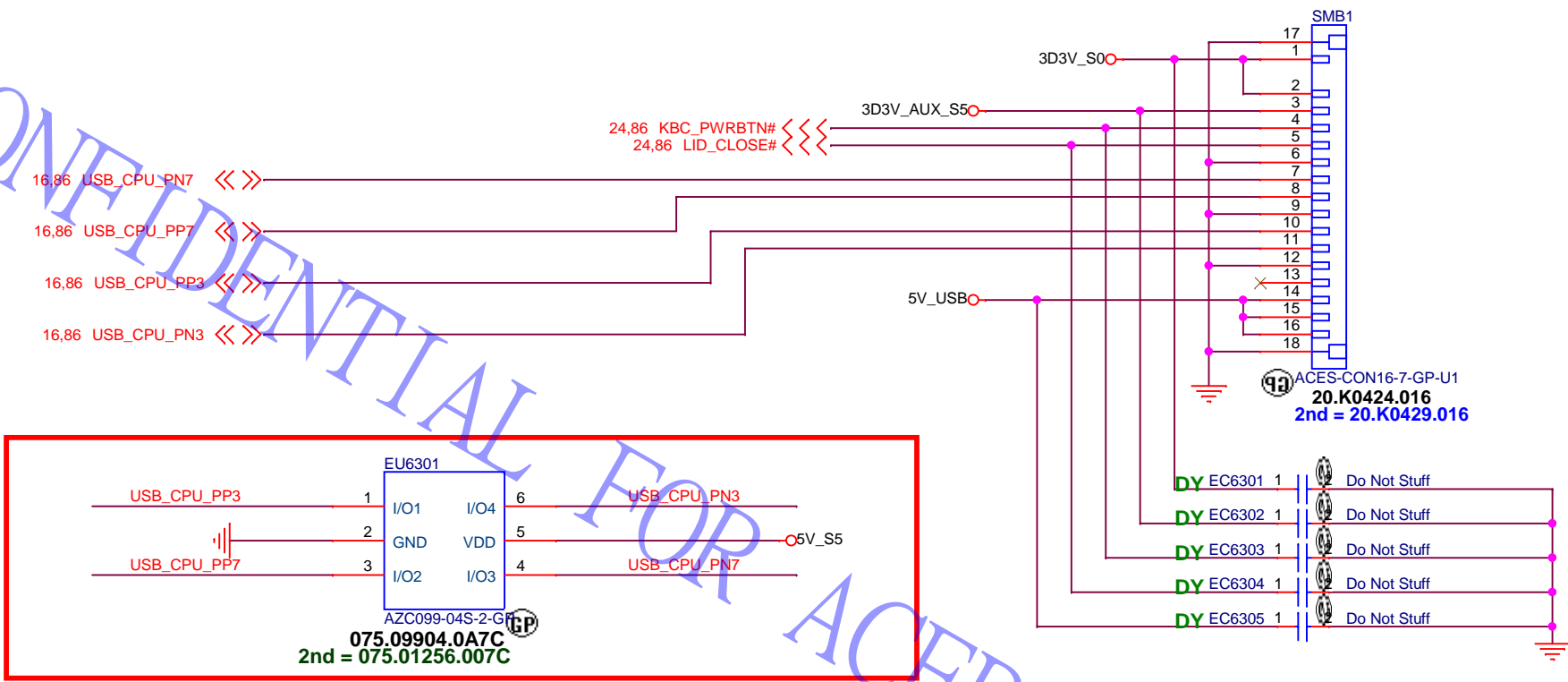
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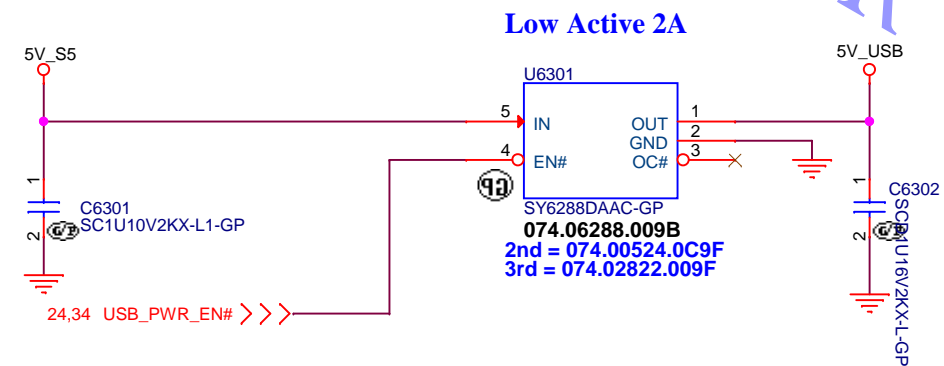
緯創資通

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Title		
Key Board/Touch Pad		
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Title			
IO Board Connector			
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Title

**Hall Sensor**

Size  
A4

Document Number

**DOMINO BH**

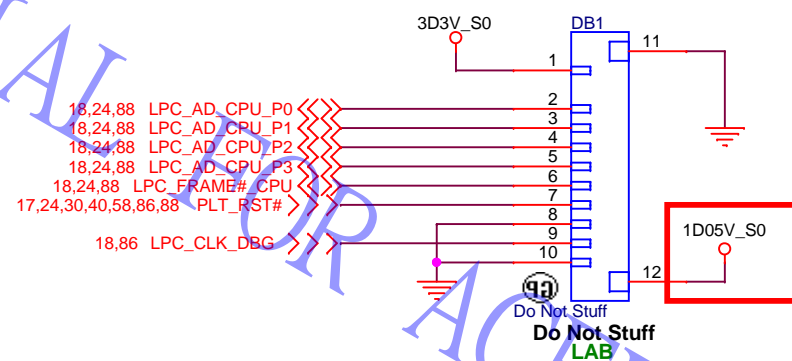
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Title

**Dubug connector**

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Size A4	Document Number <b>DOMINO BH</b>	Rev <b>-1M</b>
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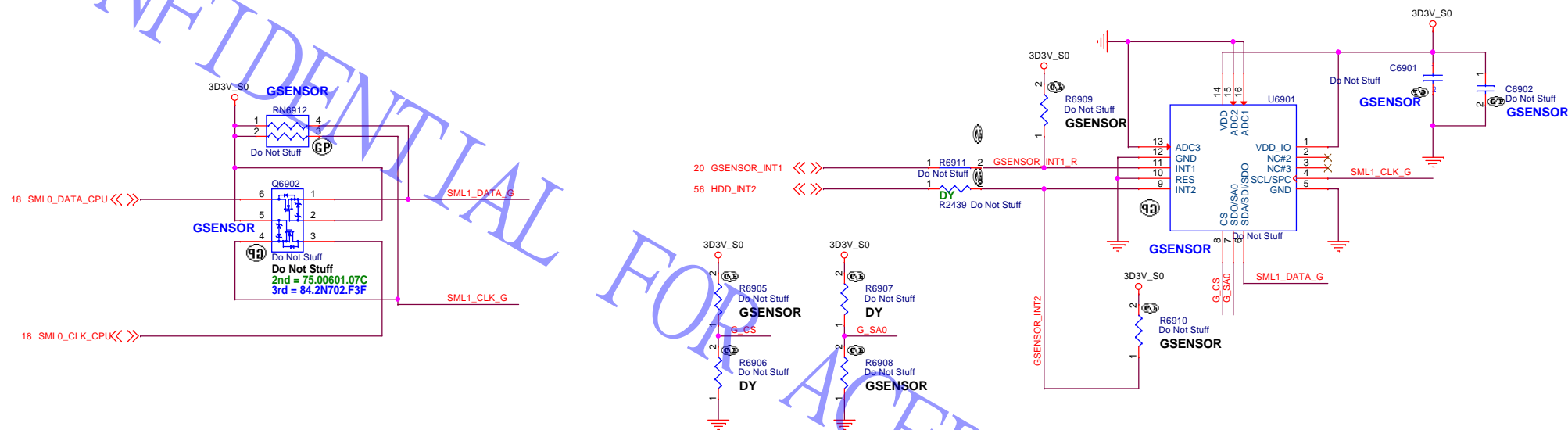
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SSID = User.Interface

## G Sensor

### Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



SDO="H"; address="3Ah"  
\*SDO="L"; address="38h"

\*CS="H"; mode="I2C"  
CS="L"; mode="SPI"

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Title		
G sensor		
Size	Document Number	Rev
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Title

**Thunderbolt (2/5)**

Size  
A4

Document Number

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Title

**Thunderbolt (4/5)**

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Title

***Thunderbolt (5/5)***

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Title

**GPU(PEG)**

Size  
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Document Number

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Rev  
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Title

**GPU (DIGITALOUT)**

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Title

**GPU (VRAM I/F)**

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Date		Title		Page	

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TitleGPU (POWER/GND)	
SizeA2	Document NumberDomino
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Title			
GPU-VRAM1,2 (1/4)			
Size	Document Number		Rev
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Title	
GPU-VRAM3,4 (2/4)	
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Title		
GPU-VRAM5,6 (3/4)		
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GPU-VRAM7,8 (4/4)		
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Title

RT8812A VGA CORE

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Title

**Switchable GFX LCD(1/2)**

Size  
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Title

**Switchable GFX LCD(2/2)**

Size  
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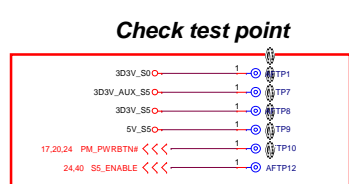
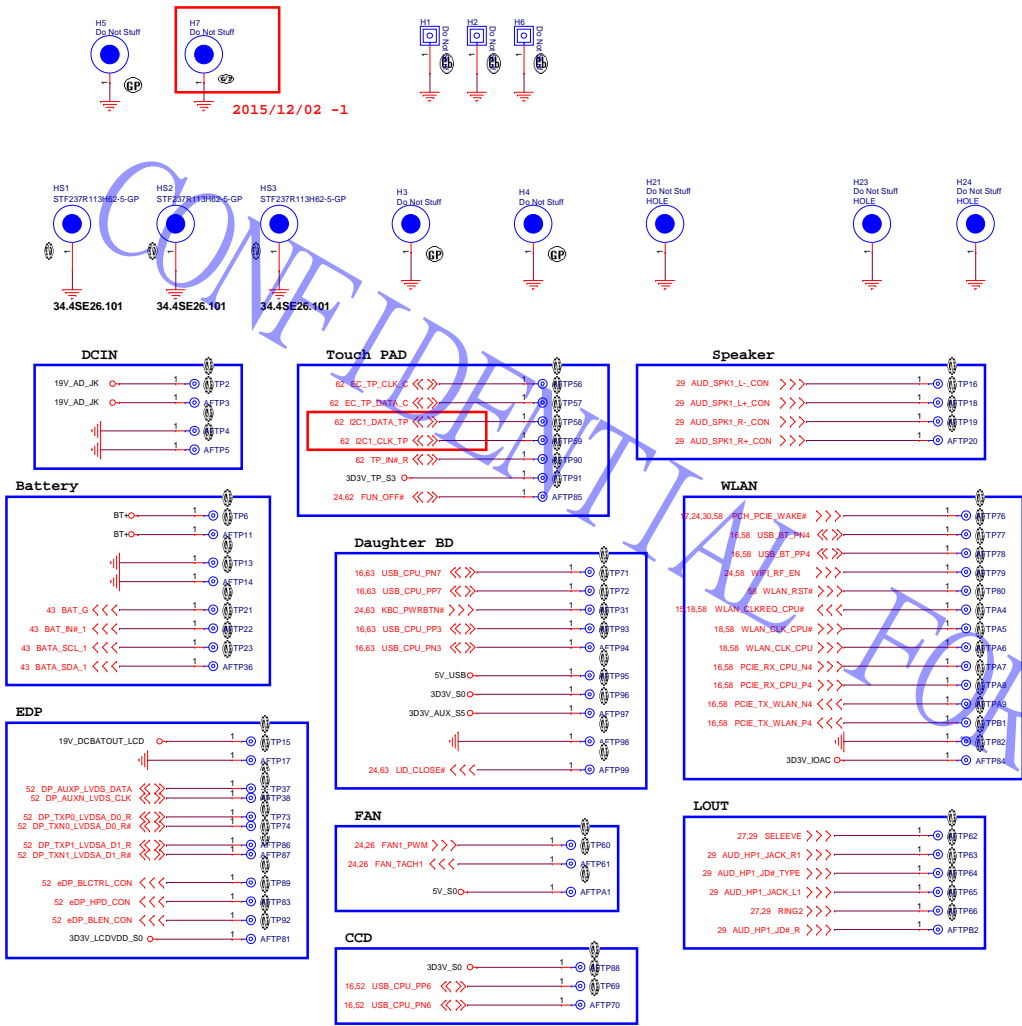
Document Number

**Domino**

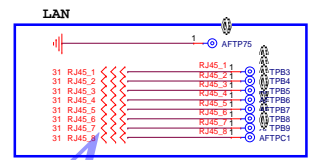
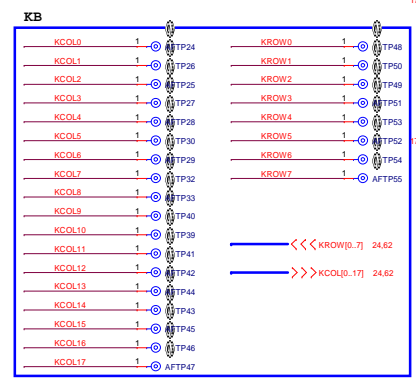
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SSID = Finger Print

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SSID = Express Card

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SSID = Smart Card

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SSID = Docking

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SSID = Intel LAN

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Title

**LAN Switch**

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Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0 <sup>1</sup>	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST# <sup>1</sup>	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4 <sup>1</sup>	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST# <sup>1</sup>	O	System	18	HOOK7	DBR# <sup>1</sup>	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH

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PCH XDP

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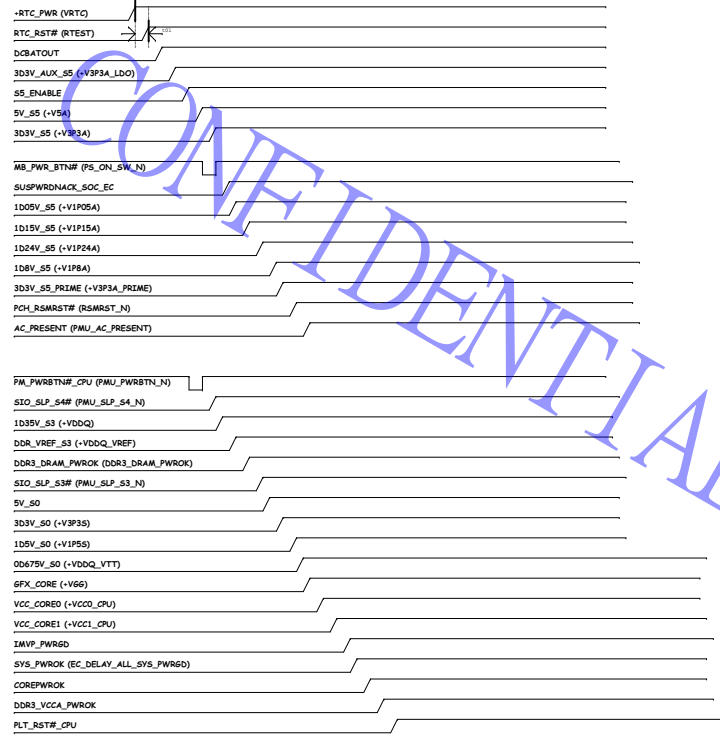
**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

**Change History**

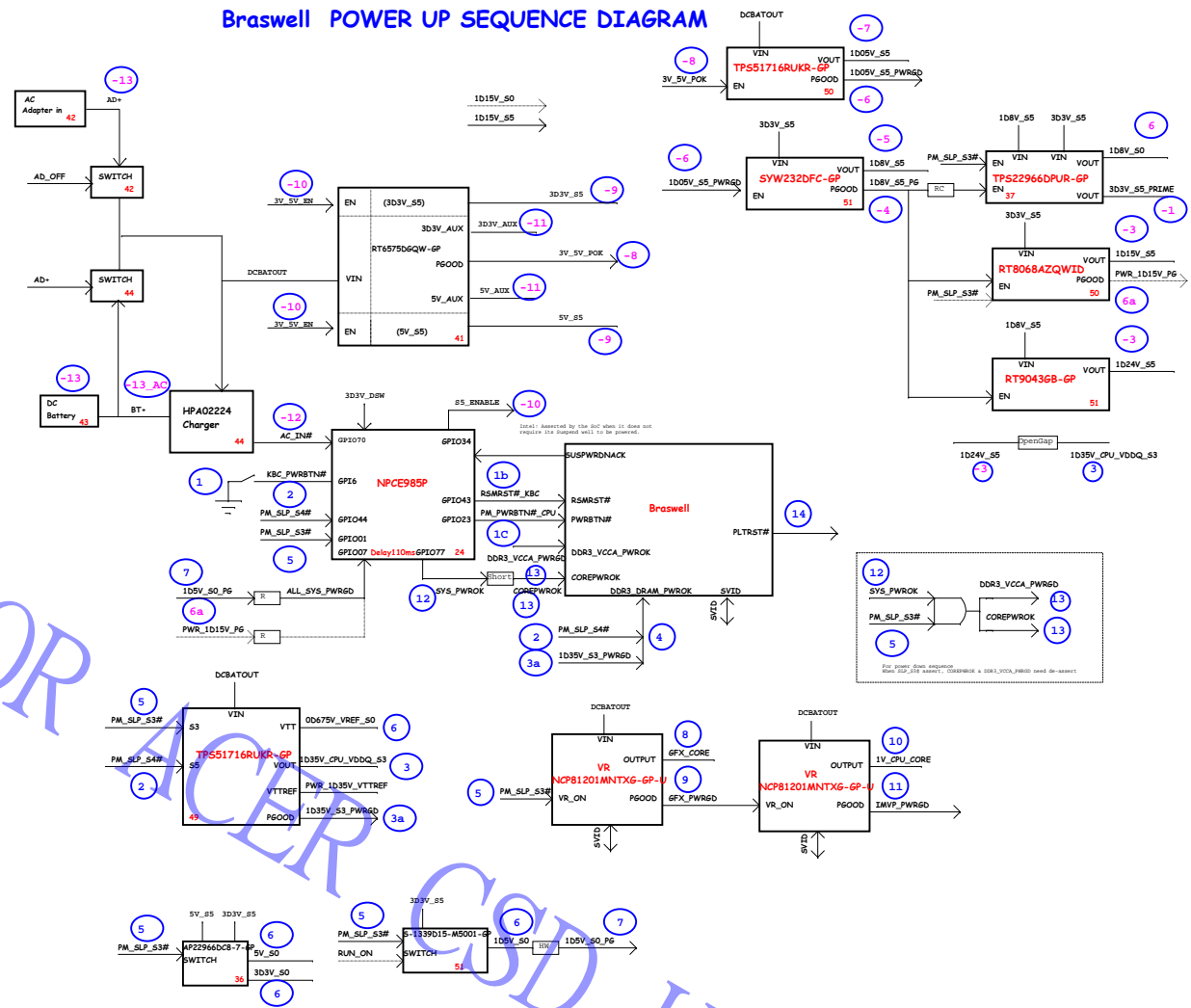
Size A4	Document Number <b>Domino</b>	Rev <b>-1</b>
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# Intel-Power Up Sequence

(AC mode)

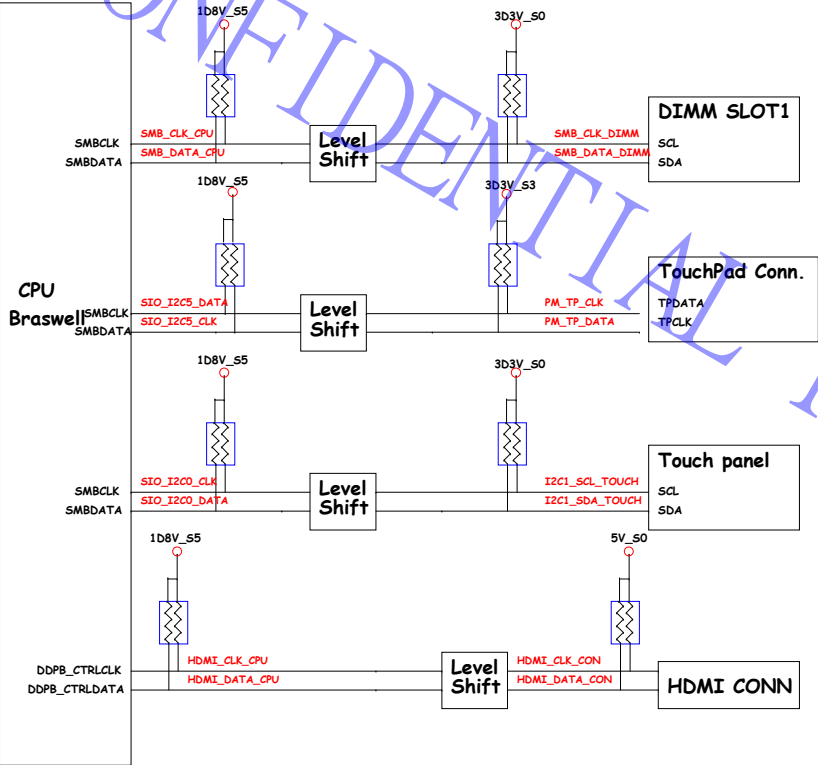


# Braswell POWER UP SEQUENCE DIAGRAM

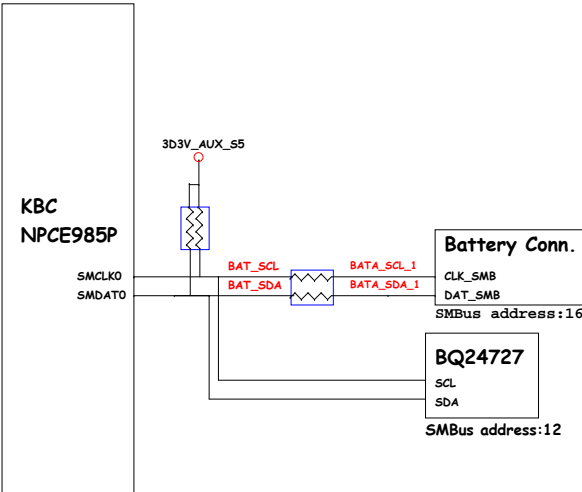




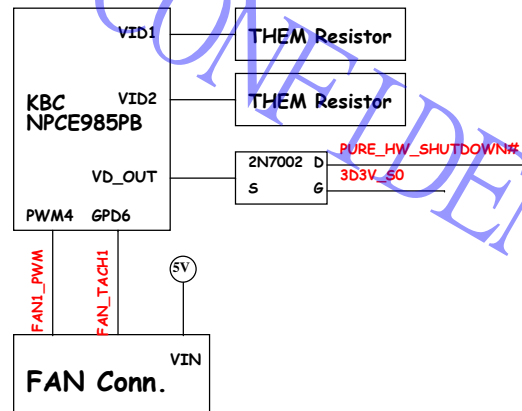
PCH SMBus Block Diagram



KBC SMBus Block Diagram



# Thermal Block Diagram



# Audio Block Diagram

